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Help | Logout | Interrupt

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

**Search Results -**

| Terms | Documents |
|---|---|
| L4 and (time$ or timing or interval or clock$) | 7 |

**Database:** US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

**Search:** L5

Refine Search

Recall Text | Clear

**Search History**

**DATE: Tuesday, April 08, 2003** Printable Copy Create Case

| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| *DB=TDBD; PLUR=YES; OP=OR* | | | |
| L5 | L4 and (time$ or timing or interval or clock$) | 7 | L5 |
| L4 | L3 and asynchronous | 8 | L4 |
| L3 | L1 and synchronous | 17 | L3 |
| L2 | L1 and syncronous | 0 | L2 |
| L1 | api or program$ adj2 interface? | 667 | L1 |

END OF SEARCH HISTORY

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**Search Results** - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: NN9702121

L5: Entry 1 of 7 File: TDBD Feb 1, 1997

TDB-ACC-NO: NN9702121

DISCLOSURE TITLE: Intelligent Miner

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☐ 2. Document ID: NN9607229

L5: Entry 2 of 7 File: TDBD Jul 1, 1996

TDB-ACC-NO: NN9607229

DISCLOSURE TITLE: Client Object Model for Distributed Servers

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☐ 3. Document ID: NN9607139

L5: Entry 3 of 7 File: TDBD Jul 1, 1996

TDB-ACC-NO: NN9607139

DISCLOSURE TITLE: Method for Keyboard Controller Support

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☐ 4. Document ID: NN9403591

L5: Entry 4 of 7 File: TDBD Mar 1, 1994

TDB-ACC-NO: NN9403591

DISCLOSURE TITLE: Ethernet Bandwidth Management

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☐ 5. Document ID: NN9207352

L5: Entry 5 of 7 File: TDBD Jul 1, 1992

TDB-ACC-NO: NN9207352

DISCLOSURE TITLE: Client Server Algorithm for Distributed Libraries.

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☐ 6. Document ID: NN9202369

L5: Entry 6 of 7 File: TDBD Feb 1, 1992

TDB-ACC-NO: NN9202369

DISCLOSURE TITLE: Platform Independent SQL Interface Architecture.

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 7. Document ID: NN86034284

L5: Entry 7 of 7 File: TDBD Mar 1, 1986

TDB-ACC-NO: NN86034284

DISCLOSURE TITLE: Directory Internal Exchange Protocol - a Generalized Protocol Mechanism for Communication Between Directory Components



Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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| Terms | Documents |
|---|---|
| L4 and (time$ or timing or interval or clock$) | 7 |

**Display Format:** TI | Change Format

Previous Page Next Page

L5: Entry 2 of 7 File: TDBD Jul 1, 1996

DOCUMENT-IDENTIFIER: NN9607229
TITLE: Client Object Model for Distributed Servers

Disclosure Text (1):
In a distributed time-independent client-server (or message-driven) environment, a client application process can send request messages to remote servers and, in general, for each request message expect to receive multiple reply messages. The needs of the application may dictate that the client process is never (or not always) blocked while it waits for replies from servers and that consequently, an arbitrarily large number of replies may be pending at any time. This introduces an administrative burden on a client application to correlate each reply with its originating request and deal with it appropriately. The interleaving of requests with replies can become complex especially when communication errors occur. Also, it cannot normally be assumed that messages (requests or replies) will arrive in the same order they were sent. While procedural APIs for client programming provide mechanisms for obtaining asynchronous replies to server requests they offer little help with their administration or the appropriate structuring of the client application. These procedural mechanisms go under names such as reply solicitation calls (with wait or nowait), callbacks, correlation identifiers and message qualifiers.

Disclosure Text (2):
Various application-specific strategies may be needed to determine when a particular client-server message-flow is complete, for example o Know how many replies to expect and just count them o Find one flagged as the last, check the sequence number on it and continue till all earlier sequence numbers have arrived o Time out o Emulate a remote procedure call; additional, but orthogonal, effort is involved in (de) marshalling in/out parameters and the procedure name o Terminate on one of a number of error conditions.

Disclosure Text (4):
A Flow object supports one of three reply synchronization models o Synchronous..the client process is blocked till the replies are received o Deferred synchronous..the process continues with other work and at some point in the future actively seeks replies. o Asynchronous..the process continues with other work but remains passively ready to be driven by the replies as they arrive. When a client application initiates a request call to a server, it references the Flow object which will control the client-server flow. It is intended that the Flow object is subclassed (specialized) by the application to implement specific reply handling behavior in a handleReply method. Different subclasses of Flow can be created to deal with different message semantics. The handleReply method is invoked by the Flow implementation when a reply is available. The timing of this depends on the synchronization model used by the particular flow; in the synchronous case the reply is handled directly the client process is unblocked when a reply arrives.

Disclosure Text (5):
For a deferred synchronous Flow, nothing happens until the client decides it is time to use the poll or wait method of Flow. If poll is used, the Flow object checks if any replies corresponding to the original server have been received. If they have, they are passed synchronously, one-by-one into the reply handler for immediate processing. If not, control returns to the client without blocking its process. For an asynchronous Flow, the replyHandler is invoked by the Flow implementation immediately the reply arrives, in parallel with whatever else the client application happens to be doing. The implementation of an asynchronous Flow requires multi-threading support.

Disclosure Text (6):
Calling the wait method of Flow temporarily turns a deferred synchronous or asynchronous Flow into a synchronous one. The client process is blocked until a reply arrives. An optional timeout value can be specified on the wait call. The reply handler has a least one input parameter which gives it access to the reply just received, and a return value indicates to the Flow implementation whether more replies are expected. Application logic added to the reply handler, together with application state instance variables added to the implementation of the subclass of Flow can be used to determine whether more replies are expected.

Disclosure Text (7):
When the client application decides a message flow is complete, the Flow object an be reused for a new message flow or destroyed. This process can be automated by a Flow Manager. If replies are to be received after an elapsed time which exceeds the lifetime of the originating application process, the FlowManager can make to Flow objects persistent. A future instance of the FlowManager can then reconstitute the hardened Flow objects and receive any pending replies. The Flow object model can be integrated with or extend the handling of the queued messages in a graphic user interface implementation.

WEST

**End of Result Set**

☐ Generate Collection Print

L5: Entry 7 of 7 File: TDBD Mar 1, 1986

DOCUMENT-IDENTIFIER: NN86034284
TITLE: Directory Internal Exchange Protocol - a Generalized Protocol Mechanism for Communication Between Directory Components

Disclosure Text (1):
- In the present description the term "directory" means a table of names and corresponding items of data. Data in a directory is locational or directive in nature, e.g., (1) a listing of names, addresses, and other data about a specific group of persons or organizations, or (2) an index that is used by a control program to locate one or more blocks of data stored in separate areas of a data set in direct access storage, or (3) an index to locate blocks of program information. The user of a directory knows the definition of the object references by a name, but needs the specific data value(s), e.g., phone number, in order to perform a specific activity. Described here is a Directory Internal Exchange Protocol which provides communications between various components of the directory or Directory Service Units (DSUs). This protocol is generalized for implementation in any data distribution scheme or network topology. This is a new concept where any transport mechanism can be employed with complete local/remote transparency. The following terms and definitions are used herein: Application Interface (API) The protocol boundary between the user and the directory service. Directory Service Interface (DSI) The internal interface between directory service units and outside services, such as communication, user services, or user data areas. Directory Service System (DSS) An instance of directory service in a given network of distributed directory services. Directory Service Unit (DSU) A unit of DSS that provides one or more directory service functions. Operations Control Block (OCB) A control block that contains directory control information. The protocol commands consist of the following two types: Request - There are a set of request commands which define the functions to be performed by receiving DSUs. Reply - There are a set of reply commands which carry the data/status resulting from processing the requested functions. A reply command will be defined with one-to-one relationship for any request command that requires a replying data/status. The status is returned to notify a request sender that a requested command completed normally or with exception. The protocol command classes are defined for the request/reply protocol as follows: No Reply Required Command Class (NRR). The NRR is used for any command that does not require a replying command from the receiver. The requester uses the NRR command class when the function requested does not require return of results/status. Only a replying command with exception condition code(s) is allowed to reply to this class of command. Such a replying command sent to NRR requests need not be synchronized or correlated. Synchronous Reply Required Command Class (SRR). The SRR is used for any command that requires a replying command as an immediate (next) command sent by the receiver. The requestor uses the SRR command class when the function requested is to be performed synchronously by the receiver and the result/status returned in a next replying command. The SRR command sender may not send another function request command until the replying command has been returned. Asynchronous Reply Required Command Class (ARR). The requestor uses the the ARR command class when the function requested need not be performed synchronously by the receiver but can be performed any time at the receiver's convenience. The ARR command sender may send another function request command before the replying command has been returned. When there are many outstanding ARR requests, the results can be returned in any order. Replying commands to the ARR commands may not be received in the order sent by the ARR receiver. Each protocol request may be uniquely identified with a command identifier (CMD_ID). The command identifiers are used to correlate the reply commands to previously sent request commands. The command identifier consists of two parts: the name of the DSU originating a request and a sequence

number. The reply command should carry the same CMD_ID as received in the request command. The command IDs are required primarily for the management of the command control blocks associated with the protocol command propagation operation. The NRR command class does not need the Command_ID since it does not require the reply and the control block is not created. The SRR command class may not need the Command_ID since only one control block exists for a single outstanding command. The ARR command class needs the Command_ID since the multiple control blocks can exist at a given time for multiple outstanding commands to be correlated with the replies. The request/reply protocol is defined to control/manage the command flows between two DSUs as a pair of the request sender and the request receiver. This protocol can be used commonly for any pair of DSUs in a DSS configuration. To illustrate the request/reply protocol, consider the following scenario: DSU(A) sends a request to DSU(B) to query a directory data; DSU(A) does not know how DSU(B) will service the request (that is, DSU(B) may be able to find the requested data from the local directory or through another DSU) and, on the other hand, DSU(B) does not know which DSU originated the query request (that is, DSU(A) may have originated the request or have sent it to service the query request from another DSU). The request must specify the command code indicating the function to be performed, any associated input data, the Command_ID and the command class specifying the request/reply protocol to be used. The reply must specify the same command code and command ID as received in the request, and the result data/status from the function performed. When the requested function does not cause the result data to be returned (for example, update), the command class is normally specified to be the NRR. However, it may specify the SRR or ARR to request for an acknowledgment with the status. The flow of the commands between two DSUs complies with the following general rules: Only one reply command is allowed for a request command. Two DSU's can send requests to each other simultaneously. When an exception condition is encountered in the processing of a command in any class, a reply command with an exception condition code will be returned in the NRR command class. The type of request/reply protocol is specified by the command class. COMMAND DESCRIPTIONS Each command description begins with the command code, the command type (request or reply), the data area to be affected (operational control block, directory descriptor, or user directory data), and a list of command specific operands. The operands basically consist of two types of information: the data description information related to data operation (for example, directory type ID, input data argument, and result data argument), and the control information related to the command protocol or propagation algorithm (for example, command class, Command_ID, origin/destination DSU name, directed/undirected, sequential/parallel, one/all result data, max hop count, and current hop count). QUERY command operates on the query propagation algorithm(s), while MODIFY, ADD, and DELETE commands operate on the update propagation algorithm(s). CREATE and RETRIEVE commands are limited to the directed operation. All other commands can operate on both directed and undirected operations. In the following command descriptions, "OCB" will be used as the abbreviation for the operational control block, "Descriptor" for the directory descriptor, and "Data" for the user directory data. The function of the command is explained, followed by a description of each operand. Optional operands are denoted by parentheses. Required Optional operands are shown without parentheses. CREATE REQUEST The CREATE request is used to build the data areas (that is, OCB, descriptor, or user directory data) for a given directory data base distributed throughout the DSS network. If the data area field indicates "OCB", this request causes the creation of an OCB at the destination DSU with the entire contents as specified in the operand. If the data area field indicates "descriptor," this request causes the creation of a directory descriptor at the destination DSU with the entire contents as specified in the operand and build a user directory data area according to the data formats specified in the descriptor. The CREATE request is under the directed operation and, therefore, it should specify the destination DSU in which the requested data area is created. Operand Description Directory Type_ID: indicates the type of directory data base. Input Data Strings: the contents of the data area to be created. Command Class: specifies the request/reply protocol. NRR/ SRR/ARR. Command_ID: unique ID assigned to the request for request/ reply correlation. If NRR specified, this field is not needed. Origin DSU Name: this is a required parameter since even in the case of NRR, the exception condition should be returned to the origin DSU. Destination DSU Name: since CREATE command performs under the directed operation, this field is a required operand to indicate which DSU the requested data area is to be created at. QUERY REQUEST The QUERY request is used to find elements of a given directory data base distributed throughout the DSS network. If the element(s) satisfying the search criteria specified by the input search argument/ data is found, the result data will be returned in the QUERY Reply. Operand Description Directory Type_ID: indicates the type of directory data base. Input Search Argument: specifies the

search argument for the input data. Input Data: specifies the actual data value to be queried for. Result Data Argument: specifies the result argument for the output data. Command Class: specifies the request/reply protocol to be used. The NRR cannot be used since the reply is always required to carry the result data for the query request. SRR/ARR Command_ID: unique ID assigned to the request for the request/reply correlation. If NRR specified, this field is not needed. Origin DSU Name: the reply is always required for the query request to return the result data, this is the required parameter. Destination DSU Name: if directed is indicated, this parameter is required. Otherwise, it is not a required parameter. Directed/Undirected: if directed is indicated, the query request will be sent to the DSU as specified in the Destination DSU Name field. If undirected is indicated, the query request will propagate according to the query propagation algorithm. Sequential/Parallel: this parameter indicates the type of the propagation mechanism to be used. Sequential propagation is a Depth First Search, whereas parallel propagation is a Breadth First Search. One/All result data: in the parallel propagation, there can be many result data arriving at a DSU. If One is indicated, only one result data will be returned on a first-come, first-serve basis to the query request sender. If All is indicated, all result data will be concatenated and returned. Max Hop Count: this is an optional parameter to be used to avoid the possible looping among the interconnected DSUs. This parameter specifies the maximum radius

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Design and Implementation of Triveni: a Process-algebraic.. - Christopher Colby (1998) (Correct) (1 citation)
and Implementation of Triveni: a Process-algebraic **API** for Threads Events Christopher Colby Lalita
Occam is based on CSP Pict is based on the (**asynchronous**) pi-calculus [16] and incorporates a powerful
such as process algebras [21, 15, 2] and **synchronous** programming languages (see [14, 4] for
www.math.luc.edu/~radha/ftp/ICCL98.ps

Improved Non-Real-Time Communication in FDDI Networks with.. - Moncef Hamdaoui (Correct)
for two types of service: **synchronous** and **asynchronous**. Each station is allocated a portion of the
provides support for two types of service: **synchronous** and **asynchronous**. Each station is allocated a
is denoted by H i .Each station has the following **timers**/counters: 1. Token Rotation **Timer** (TRT)TRT
ftp.ece.wisc.edu/pub/parmesh/conferences/aperiodic.ps.gz

Asynchronous Design Methodologies: An Overview - Hauck (1995) (Correct) (51 citations)
IEEE, Vol. 83, No. 1, pp. 69-93, January, 1995. **Asynchronous** Design Methodologies: An Overview Scott
no need to worry about clock skew. In contrast, **synchronous** systems often slow down their circuits to
www.ece.nwu.edu/~hauck/publications/AsynchArt.ps

Medium Access Control for Synchronous Traffic in the AMNET LAN - David Goodall (Correct)
48 bytes of data to maintain compatibility with **Asynchronous** Transfer Mode (ATM) cells from the adaptation
Medium Access Control For **Synchronous** Traffic In The Amnet Lan David Goodall
ftp.cse.unsw.edu.au/pub/doc/papers/UNSW/9501.ps.Z

A Proposal for Research on the Testability of Asynchronous Circuits - Liebelt (1998) (Correct)
A Proposal for Research on the Testability of **Asynchronous** Circuits Michael Liebelt August 25, 1998
www.eleceng.adelaide.edu.au/Groups/CHIPTEC/papers/HPCA-ECS-96-01.ps

On Non-existence of Optimal Local Synchronous Bandwidth.. - Ching-Chih Han (1995) (Correct) (2 citations)
messages into two classes: **synchronous** and **asynchronous**. **Synchronous** messages arrive at regular
On Non-existence of Optimal Local **Synchronous** Bandwidth Allocation Schemes for the
it arrives early .Specifically, each node has two **timers** and one counter: ffl The token rotation **timer**
eewww.eng.ohio-state.edu/drcl/papers/ipccc95.ps

Applying The Proactor Pattern To High-Performance Web Servers - James Hu (1998) (Correct) (4 citations)
I/O functions are provided by the aio family of **APIs** [17]In Windows NT, I/O completion ports and
increasing number of operating systems support **asynchronous** mechanisms that provide the benefits of
128.252.165.44/~schmidt/PDCS-98.ps.gz

RTL Verification of Timed Asynchronous and Heterogeneous.. - Vakilotojar, Beerel (1997) (Correct)
RTL Verification of Timed **Asynchronous** and Heterogeneous Systems using Symbolic Model
are a network of communicating **asynchronous** and **synchronous** components and have correctness
constraints
We encode passage of time using explicit **timers** for ab ceba -c-e-be ceb -c-ec
jungfrau.usc.edu/pub/aspdac97_w_corr.ps

An Asynchronous to Synchronous Interface for a B-ISDN.. - Rushan Muttucumaru (Correct)
An **Asynchronous** to **Synchr nous** Interface for a B-ISDN
An **Asynchr nous** to **Synchronous** Interface for a B-ISDN Customer Switching
www.elec.uow.edu.au/conferences/95-140.ps

An Efficient and Practical Synchronous Bandwidth Allocation Scheme .. - Zhang (Correct)

into two types: **synchronous** messages and **asynchr nous** messages. **Synchr nous** messages, such as
An Efficient and Practical **Synchr n us** Bandwidth Allocation Scheme for Deadline
www.cs.york.ac.uk/ftpdir/reports/YCS-95-255.ps.Z

Efficient Symbolic Detection of Global Properties in.. - Scott Stoller (1998) (Correct) (1 citation)
for detecting whether a computation of an **asynchron us** distributed system satisfies Poss \Phi (read
[FR97] or assuming that the system is partially **synchron us** [MN91,Sto97]This paper presents an efficient
a specified initial state and optionally with its **timer** set to a specified value. Computations contain
ftp.cs.indiana.edu/pub/stoller/CAV98.ps

Asynchronous Transpose-Matrix Architectures - Tierno, Kudva (1997) (Correct) (1 citation)
**Asynchronous** Transpose-Matrix Architectures Jos'e A.
relative advantages of each one. 1 Introduction **Synchronous** pipelines are used widely in DSP applications,
www.cs.utah.edu/~ganesh/w97-asic/pk-paper.ps

CoReA: a Synchronous Calculus of Parallel Communicating Reactive.. - Boniol (1994) (Correct)
safety, concurrency and determinism. Several **asynchronous** or strong **synchronous** answers have been
et de l'Espace `a Toulouse CoReA: a **Synchronous** Calculus of Parallel Communicating Reactive
ftp.cert.fr/pub/SATURNE/PARLE94_vf.ps

Object Interconnections - Programming Asynchronous (Correct)
Object Interconnections Programming **Asynchronous** Method Invocations with CORBA Messaging
the tedium of programming with deferred **synchronous** operations via the Dynamic Invocation
www-irl.iona.com/hyplan/vinoski/col16.ps.Z

Chan: an Asynchronous Data-Parallel Language for Irregular.. - Emmanuel Melin (Correct)
SCL \Gamma Chan: an **Asynchronous** Data-Parallel Language for Irregular
new programming language that integrates both a **synchronous** data-parallel programmingmodel and an
web.univ-orleans.fr/SCIENCES/LIFO/Membres/melin/PAPERS/PAPERS/hips97.ps.Z

A High-Performance Asynchronous SCSI Controller - Yun, Dill (1995) (Correct) (7 citations)
A High-Performance **Asynchronous** SCSI Controller Kenneth Y. Yun Department of
internal events. Such components are called **synchronous** circuits. On the other hand, system components
sprout.stanford.edu/PAPERS/YD95.ps

High-Performance Asynchronous Pipeline Circuits - Kenneth Yun (1996) (Correct) (4 citations)
High-Performance **Asynchronous** Pipeline Circuits Kenneth Y. Yun Department
functional units previously designed for use in **synchronous** circuits. Micropipelines is based on a
paradise.ucsd.edu/PAPERS/ASYNC-96.ps

Average-Case Optimized Technology Mapping of One-Hot Domino.. - Wei-Chun Chou (1998) (Correct)
(4 citations)
for optimizing the average-case delay of **asynchronous** combinational circuits implemented using
circuits are attractive alternatives to **synchronous** circuits because they have the potential
paradise.ucsd.edu/PAPERS/ASYNC-98-DOMINO.ps

Architecture for Synchronous Groupware Application Development - Balter (1995) (Correct) (1 citation)
open applications. An open application provides an **API** (Application Programming Interface) mechanism
are the interaction scheme (**synchronous** versus **asynchronous**)the architecture (centralized, replicated or
HCI'95 -July 1995 Tokoy Japan Architecture for **Synchronous** Groupware Application Development Roland
ftp.inrialpes.fr/pub/INRIA/projets/SIRAC/publications/95-hci-coopscan-PUB.ps.gz

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(4)

# SEARCH REQUEST FORM

**Scientific and Technical Information Center**

Requester's Full Name: Diem Ky Cao Examiner #: 79422 Date: 4/1/03
Art Unit: 2126 Phone Number 305-5220 Serial Number: 09/675,545
Mail Box and Bldg/Room Location: CPK2-5A06 (CPK2-5A04) Results Format Preferred (circle): PAPER DISK E-MAIL

**If more than one search is submitted, please prioritize searches in order of need.**

**********

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: Efficient Timer management system

Inventors (please provide full names): Philippe Damon, Marco C. Hedges

Earliest Priority Filing Date: 9/28/2000

***For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.**

A timer management system in both synchronous and asynchronous system. Application program interface (API) and state machine are used to manipulate timer object.

**********

| STAFF USE ONLY | Type of Search | Vendors and cost where applicable |
|---|---|---|
| Searcher: Dao-Ho Holloway | NA Sequence (#) | STN |
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| Clerical Prep Time: | Patent Family | WWW/Internet ✓ |
| Online Time: 240 | Other | Other (specify) |

PTO-1590 (1-2000)

```
Set     Items   Description
S1      32723   API OR APPLICATION()PROGRAM?()INTERFACE? OR (APPLICATION? -
             OR PROGRAM?)(2W)INTERFACE?
S2      22347   (TIME()DEPENDENT? OR SYNCHRON?) AND (ASYNCHRON? OR (NON OR
             "NOT")()SYNCHRONOUS)
S3     769464   TIMER? OR TIMING OR TIMESTAMP? OR INTERVAL? OR CLOCK?
S4     962212   END? ? OR TIMEOUT? OR TIME()OUT? ? OR EXPIR?
S5       1547   S3(3N)(DATABASE? OR DATA()(BASE? OR BANK? OR FILE?) OR DAT-
             ABANK? OR DATAFILE? OR TABLE?)
S6     298059   STATEMACHINE? OR STATE()MACHINE? OR CONTROLLER?
S7        627   INITILIALI? OR REINITIALI?
S8      26199   S3(3N)(MANAG? OR CONTROL? OR ADMINIST? OR MONITOR? OR TRAC-
             K?)
S9          0   S1 AND S2 AND S5 AND S8
S10         8   S1 AND S5
S11         4   S1 AND S2 AND S8
S12       114   S1 AND S2
S13         1   S12 AND S3 AND S4
S14        11   S12 AND S3
S15         0   S12 AND S6 AND S7
S16         0   S12 AND S7
S17         7   S12 AND S6
S18        26   S10 OR S11 OR S13 OR S14 OR S17
S19        21   RD (unique items)
S20        21   S19 NOT PY>2000
S21        21   S20 NOT PD>20000928
File   8:Ei Compendex(R) 1970-2003/Mar W5
         (c) 2003 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2003/Mar
         (c) 2003 ProQuest Info&Learning
File  65:Inside Conferences 1993-2003/Apr W1
         (c) 2003 BLDSC all rts. reserv.
File   2:INSPEC 1969-2003/Mar W5
         (c) 2003 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2003/Apr W1
         (c)2003 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2003/Apr 03
         (c) 2003 The Gale Group
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         (c) 2003 Info. Today Inc.
File 144:Pascal 1973-2003/Mar W5
         (c) 2003 INIST/CNRS
File  34:SciSearch(R) Cited Ref Sci 1990-2003/Mar W5
         (c) 2003 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/Feb
         (c) 2003 The HW Wilson Co.
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**21/5/1 (Item 1 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)


06335696 E.I. No: EIP03137412854
**Title: The timely computing base: Timely actions in the presence of uncertain timeliness**
Author: Verissimo, Paulo; Casimiro, Antonio; Fetzer, Christof
Conference Title: Proceedings of the International Conference on Dependable Systems and Networks
Conference Location: New York, NY, United States Conference Date: 20010701-20010704
Sponsor: IEEE Computer Society (TCFTC); IFIP Working Group 10.4 on Dependable Comp. and Fault Tolerance
E.I. Conference No.: 60558
Source: Proceedings of the 2002 International Conference on Dependable Systems and Networks 2000.
Publication Year: 2000
ISBN: 0769507085
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); T ; (Theoretical)
Journal Announcement: 0303W5
Abstract: Real-time behavior is specified in compliance with timeliness requirements, which in essence calls for **synchronous** system models. However, systems often rely on unpredictable and unreliable infrastructures, that suggest the use of **asynchronous** models. Several models have been proposed to address this issue. We propose an architectural construct that takes a generic approach to the problem of programming in the presence of uncertain timeliness. We assume the existence of a component, capable of executing timely functions, which helps applications with varying degrees of **synchrony** to behave reliably despite the occurrence of **timing** failures. We call this component the Timely Computing Base; TCB. This paper describes the TCB architecture and model, and discusses the **application programming interface** for accessing the TCB services. The implementation of the TCB services uses fail-awareness techniques to increases the coverage of TCB properties. 22 Refs.
Descriptors: Fault tolerant computer systems; Real time systems; Mathematical models; Systems analysis; Computer **programming** ; **Interfaces** (computer); Surveys
Identifiers: Timely computing base; **Synchronous** system models; **Application programming interface**
Classification Codes:
722.4 (Digital Computers & Systems); 921.6 (Numerical Methods); 723.1 (Computer Programming); 722.2 (Computer Peripheral Equipment)
722 (Computer Hardware); 921 (Applied Mathematics); 723 (Computer Software, Data Handling & Applications)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

**21/5/2 (Item 2 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)


04272260 E.I. No: EIP95072797917
**Title: Using events to build distributed applications**
Author: Bacon, Jean; Bates, John; Hayton, Richard; Moody, Ken
Corporate Source: Univ of Cambridge Computer Lab, Cambridge, Engl
Conference Title: Proceedings of the 2nd International Workshop on Services in Distributed and Networked Environments
Conference Location: Whistler, BC, Can Conference Date: 19950605-19950606
Sponsor: IEEE
E.I. Conference No.: 43317
Source: Proceedings of the International Workshop on Services in Distributed and Networked Environments 1995. IEEE, Los Alamitos, CA, USA,95TH8091. p 148-155

Publication Year: 1995
CODEN: 85OYA3
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications)
Journal Announcement: 9512W3
Abstract: We have extended an Interface Definition Language to handle event registration and notification. Clients register interest in specified classes of events and servers then notify them of any occurrence **asynchronously** . Event occurrences are identified by parameters which conform to IDL typing constraints and can therefore be used in **synchronous** method invocations. Methods to handle registration and notification are generic and can be inherited by objects of any class: as a by-product of IDL processing the stubs to handle event creation and decoding are generated automatically. We have implemented a prototype composite event recogniser based on non-deterministic finite **state machines** . Initial experience with this prototype is encouraging. (Author abstract) 9 Refs.
Descriptors: Distributed computer systems; Object oriented programming; Computer **programming** languages; **Interfaces** (computer); Computer networks; Finite automata; Decoding
Identifiers: Interface definition language; Event registration; **Synchronous** method invocations; Prototype composite event recogniser; Finite **state machine**
Classification Codes:
723.1.1 (Computer Programming Languages)
722.4 (Digital Computers & Systems); 723.1 (Computer Programming); 722.2 (Computer Peripheral Equipment); 722.3 (Data Communication, Equipment & Techniques); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory)
722 (Computer Hardware); 723 (Computer Software); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING)

**21/5/3 (Item 3 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)


04070050 E.I. No: EIP95022559988
**Title: Self timed interrupt** controller : **a case study in** asynchronous **micro-architecture design**
Author: De Gloria, Alessandro; Faraboschi, Paolo; Olivieri, Mauro
Corporate Source: Univ of Genoa, Genoa, Italy
Conference Title: Proceedings of the 7th IEEE International ASIC Conference and Exhibit
Conference Location: Rochester, NY, USA Conference Date: 19940919-19940923
E.I. Conference No.: 42410
Source: Annual IEEE International ASIC Conference and Exhibit 1994. IEEE, Piscataway, NJ, USA,94TH0685-8. p 296-299
Publication Year: 1994
CODEN: PIAEF2 ISSN: 1063-0988
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications)
Journal Announcement: 9504W3
Abstract: We report the results of the design and layout simulation of an interrupt **controller** dedicated to the SGS-Thomson ST9 microprocessor family. The unit is composed of a delay insensitive local control-path and a **synchronous** local data-path for priority computations. The local control-path is automatically synthesized out of an Occam algorithmic specification, while the local data-path is made up of conventional hardware units. Layout simulation shows that the average time for an interrupt to be served is reduced to 28%. (Author abstract) 18 Refs.
Descriptors: Computer simulation; Integrated circuit layout; Computer architecture; Microprocessor chips; Algorithms; Computational methods; Computer hardware; Computer software; Computer **programming** languages; User **interfaces**
Identifiers: Self timed interrupt **controller** ; **Asynchronous** circuits; Central processing unit; **Asynchronous** micro architecture design; Occam

algorithmic specification
Classification Codes:
723.1.1 (Computer Programming Languages)
723.5 (Computer Applications); 714.2 (Semiconductor Devices & Integrated Circuits); 921.6 (Numerical Methods); 722.4 (Digital Computers & Systems); 723.1 (Computer Programming)
723 (Computer Software); 714 (Electronic Components); 921 (Applied Mathematics); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS)

**21/5/4 (Item 4 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)


03618625 E.I. No: EIP93030724641
**Title: Integration of a database system with real-time kernel for time-critical applications**
Author: Son, Sang H.; Yannopoulos, Stavros; Kim, Young-Kuk; Iannacone, Carmen C.
Corporate Source: Univ of Virginia, Charlottesville, VA, USA
Conference Title: Proceedings of the Second International Conference on Systems Integration - ICSI'92
Conference Location: Morristown, NJ, USA Conference Date: 19920615
Sponsor: IEEE
E.I. Conference No.: 17983
Source: Proceedings of the Second International Conference on Systems Integration Proc Second Int Conf Syst Integr ICSI 92 1992. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p 172-180
Publication Year: 1992
ISBN: 0-8186-2697-6
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); X ; (Experimental)
Journal Announcement: 9306W2
Abstract: Transactions in real-time database systems should be scheduled considering both data consistency and **timing** constraints. Since a **database** system must operate in the context of available operating system services, an environment for database systems development must provide facilities to support operating system functions and integrate them with database systems for experimentation. We chose the ARTS real-time operating system kernel. In this paper we present our experience in integrating a relational database manager with a real-time operating system kernel and our attempts at providing flexible control for concurrent transaction management. Current research issues involving the development of a **programming interface** and imprecise computing server are also discussed. (Author abstract) Refs.
Descriptors: *Relational database systems; Real time systems; Computer operating systems; Distributed computer systems; Computer programming; Computer aided software engineering; Computer networks; Scheduling; Database systems
Identifiers: Systems integration; Database transactions; Real time operating systems; Relational database manager; Servers; Programming environments
Classification Codes:
723.3 (Database Systems); 723.1 (Computer Programming)
723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

**21/5/5 (Item 5 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)


03510988 E.I. Monthly No: EIM9211-054866
**Title: Design of a data acquisition system based on the decommutation of an embedded** asynchronous **data stream without primary and secondary frame**

synchronization .
Author: Kvasnak, Michael A.; Koonmen, James P.; Grajeda, Vivian L.
Corporate Source: Phillips Lab, Kirtland AFB, NM, USA
Conference Title: 27th International Telemetric Conference - ITC/USA '91
Conference Location: Las Vegas, NV, USA Conference Date: 19911104
Sponsor: Int Foundation for Telemetering
E.I. Conference No.: 15709
Source: International Telemetering Conference (Proceedings) v 27. Publ by Int Foundation for Telemetering, Woodland Hills, CA, USA. p 27-36
Publication Year: 1991
CODEN: ITCOD6 ISSN: 0884-5123 ISBN: 1-55617-329-6
Language: English
Document Type: PA; (Conference Paper) Treatment: T; (Theoretical); X; (Experimental)
Journal Announcement: 9211
Abstract: The use of embedded **asynchronous** data streams is becoming a popular means of expanding existing telemetry systems and acquiring subsystem data. In such systems, **synchronization** between the primary and secondary system(s) **clocks** is usually considered a prerequisite. The Phillips Laboratory has developed a software/hardware approach to the problem of decommutating an embedded **asynchronous** data stream without primary and secondary frame and **clock synchronization** . The methodology employed is easily implemented and adapted to many system configurations, and represents a low-cost option in the acquisition of subsystem data. More importantly, the use of such a system greatly reduces the amount of systems integration effort required to incorporate multiple subsystems into a host telemetry system. (Author abstract) 4 Refs.
Descriptors: DATA PROCESSING--*Data Acquisition; TELEMETERING--Computer Applications; COMPUTER HARDWARE--Applications; COMPUTER SOFTWARE--**Applications** ; COMPUTER **INTERFACES** --Applications; COMPUTER ARCHITECTURE
Identifiers: EMBEDDED **ASYNCHRONOUS** DATA STREAM; PRIMARY/SECONDARY DATA **CLOCKS** ; SYSTEM ARCHITECTURE TRADE STUDIES; LOGIC STRUCTURE; DATA DISCONTINUITY
Classification Codes:
723 (Computer Software); 722 (Computer Hardware); 716 (Radar, Radio & TV Electronic Equipment); 718 (Telephone & Line Communications); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

**21/5/6 (Item 6 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)


03053693 E.I. Monthly No: EIM9104-017610
**Title: Architectural considerations for a generic multi-port digital interface.**
Author: Chimene, Mark C.
Corporate Source: Rockwell Int Missile Systems Div
Conference Title: International Telemetering Conference - ITC/USA '90
Conference Location: Las Vegas, NV, USA Conference Date: 19901029
Sponsor: Int Foundation for Telemetering; ISA
E.I. Conference No.: 14261
Source: International Telemetering Conference (Proceedings) v 26. Publ by Int Foundation for Telemetering, Woodland Hills, CA, USA. p 631-634
Publication Year: 1990
CODEN: ITCOD6 ISSN: 0884-5123
Language: English
Document Type: PA; (Conference Paper) Treatment: A; (Applications)
Journal Announcement: 9104
Abstract: Telemetry system requirements are driven by technological developments in other areas, thus the capabilities of one are mirrored in the capabilities of the other. Contemporary systems typically involve two or more digital subsystems, each operating at a unique **clock** rate. Complete **synchronization** is seldom realized in discrete systems. Because the Telemetry system must provide information sufficient to isolate data/process corruption, it must accept data from the various subsytems at different rates and times. What is needed is a technique to de-couple the

Telemetry system **clock** rate from that of the Subject system or any of its subsystems. This technique must bridge the gap between the **synchronous** data transmission fundamental to the Telemetry system and the **asynchronous** data transfer required by the various nonintegrated subsystems. This paper will discuss the design challenges offered by such a Subject system for both real time and post flight analysis. It will discuss how the restrictions imposed by the IRIG standards and anticipated mission requirements factored into developing the architecture for a Generic Multi-Port Digital Telemetry Interface.
Descriptors: TELEMETERING SYSTEMS--*Computer **Applications** ; COMPUTER **INTERFACES**
Identifiers: DIGITAL INTERFACES
Classification Codes:
716 (Radar, Radio & TV Electronic Equipment); 718 (Telephone & Line Communications); 723 (Computer Software); 722 (Computer Hardware)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

**21/5/7 (Item 7 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)


02989022 E.I. Monthly No: EI9012143503
**Title: Simplify a RISC embedded-controller interface using a PLD.**
Author: Bowns, Thom
Corporate Source: Intel Corp, Folsom, CA, USA
Source: Electronic Design v 38 n 2 Jan 25 1990 7p
Publication Year: 1990
CODEN: ELODAW ISSN: 0013-4872
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)
Journal Announcement: 9012
Abstract: Designers are turning to reduced-instruction-set computer (RISC) processors, such as the 80960KB, for embedded-control systems because they deliver the necessary speed and streamlined operation. Design problems arise, however, when RISC processors are used. For example, RISC processors have more complex interface needs than do slower, conventional embedded controllers. With the 80960KB, designers can take advantage of the 85C960 programmable-logic device, which implements the difficult portions of the interface and easily configures the programmable logic. The difficult portions that are handled by the application-specific PLD include the burst logic and timing control with all of their state **tables** , **timing** analysis, and logic design. The programmable logic implements flexible address decode and complete wait-state coverage.
Descriptors: LOGIC DEVICES--* **Applications** ; COMPUTER **INTERFACES** ; LOGIC DESIGN; COMPUTER ARCHITECTURE--Reduced Instruction Set Computing
Identifiers: RISC EMBEDDED-CONTROLLER INTERFACE; PROGRAMMABLE LOGIC DEVICES(PLD); BURST LOGIC; TIMING CONTROL; TIMING ANALYSIS
Classification Codes:
721 (Computer Circuits & Logic Elements); 722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

**21/5/8 (Item 8 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)


02734439 E.I. Monthly No: EI8904034646
**Title: Representation of control and timing behavior with applications to interface synthesis.**
Author: Hayati, Sally A.; Parker, Alice C.; Granacki, John J.
Corporate Source: Univ of Southern California, Los Angeles, CA, USA
Conference Title: 1988 IEEE International Conference on Computer Design: VLSI in Computers & Processors (ICCD '88), Proceedings
Conference Location: Rye Brook, NY, USA Conference Date: 19881003
Sponsor: IEEE, Computer Soc, Los Alamitos, CA, USA; IEEE, Circuits &

Systems Soc, New York, NY, USA; IEEE, Electron Devices Soc, New York, NY, USA
E.I. Conference No.: 11897
Source: 1988 IEEE Int Conf Comput Des VLSI Comput Process ICCD 88 Proc. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (cat n 88CH2643-5) Piscataway, NJ, USA. p 382-387
Publication Year: 1988
ISBN: 0-8186-0872-2
Language: English
Document Type: PA; (Conference Paper) Treatment: T; (Theoretical)
Journal Announcement: 8904
Abstract: The authors describe a formalism for the representation of interface behavior which can be used for high-level synthesis by a design automation system. The Design Data Structure can represent the many facets of interface behavior in a unified way, including **timing** constraints, **synchronous** and **asynchronous** signals, control flow, and data manipulation. Its descriptive power is more complete than some other formalisms in use, including event and annotated data-flow graphs. The representations described here can be used by data path synthesizers to capture more complex **timing** information than is typically handled and to separate control from data manipulation information to produce cleaner data flow graphs. The Design Data Structure has been used successfully as an internal representation for a natural-language interface for system specification. 11 Refs.
Descriptors: *INTEGRATED CIRCUITS, VLSI--*Synthesis; COMPUTER AIDED DESIGN
Identifiers: INTERFACE CIRCUITS; **TIMING** BEHAVIOR; **CONTROL** BEHAVIOR; DESIGN DATA STRUCTURE; DATA PATH SYNTHESIZERS
Classification Codes:
713 (Electronic Circuits); 723 (Computer Software)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

**21/5/9 (Item 9 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)


00830347 E.I. Monthly No: EI7907050836 E.I. Yearly No: EI79023085
**Title: AT LAST! A DATA-COMM INTERFACE CHIP THAT REALLY UNLOADS YOUR CPU -- EVEN IN BISYNC.**
Author: Cole, Everet W.
Corporate Source: Signetics Corp, Sunnyvale, Calif
Source: Electronic Design v 27 n 8 Apr 12 1979 p 100-104
Publication Year: 1979
CODEN: ELODAW ISSN: 0013-4872
Language: ENGLISH
Journal Announcement: 7907
Abstract: An enhanced **programmable** communications **interface** chip can support all popular character-oriented **synchronous** data-link procedures, including character-controlled ANSI 3. 28, ISO 1745 and -- notably -- IBM's BISYNC protocol with far less CPU intervention than any similar previous chip. The interface consists of a line **controller** , which handles **asynchronous** and **synchronous** data on CPU command, and a companion cyclic-redundancy-check generator.
Descriptors: *DATA TRANSMISSION EQUIPMENT; COMPUTERS, DIGITAL--Data Communication Equipment
Classification Codes:
718 (Telephone & Line Communications); 722 (Computer Hardware)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

**21/5/10 (Item 1 from file: 35)**
DIALOG(R)File 35:Dissertation Abs Online


01423175 ORDER NO: AADAA-I9520896
**PHASED LOGIC: A DESIGN METHODOLOGY FOR DELAY-INSENSITIVE,** SYNCHRONOUS **CIRCUITRY**

Author: LINDER, DANIEL HOOD
Degree: PH.D.
Year: 1994
Corporate Source/Institution: MISSISSIPPI STATE UNIVERSITY (0132)
Major Professor: JAMES C. HARDEN
Source: VOLUME 56/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 1614. 208 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL; COMPUTER SCIENCE
Descriptor Codes: 0544; 0984

Phased logic is proposed as a solution to the growing problem of **timing** complexity in digital design. Sources of this complexity include the increase in wire propagation delays relative to gate delays and the difficulty of high-frequency, low-skew **clock** distribution. To satisfy **timing** constraints in the context of these problems, the logic designer must increasingly analyze and modify a circuit's physical implementation. Phased logic is a delay-insensitive design methodology that restores the separation between logical and physical design by reducing **timing** complexity. No propagation delays must be calculated, and no **clock** signals are needed. However, unlike **asynchronous** methodologies that also avoid **clocks** , phased logic remains **synchronous** . Instead of requiring the designer to learn a fundamentally new design paradigm, phased logic supports the same cyclic, deterministic behavior associated with **clocked** systems. This permits the designer to rely on his previous experience and CAD tools to create phased logic systems. Phased logic also has a predictable worst-case performance that makes real-time **applications** and **interfaces** to **clocked** circuitry possible.

To escape the limitations of regular gates in delay-insensitive design, phased logic uses gate primitives that operate directly on LEDR encoded signals. Marked graph theory provides a framework for governing interconnections of these primitives so that large, complex networks of gates behave in an overall delay-insensitive, **synchronous** fashion. The primitives can be used directly in gate topologies generated by CAD tools for **clocked** systems, but a small percentage of new signals and gates must be added to guarantee delay-insensitivity. An algorithm is developed for making these additions and is tested on benchmark circuits. To obtain realistic values for speed and area, a CMOS layout is created for a programmable gate similar to those found in FPGAs. The speed of the programmable gate is comparable to **clocked** gates of similar functionality, but the area is expanded by a factor of four due to the LEDR encoding. Although phased logic requires additional circuitry, it promises to significantly decrease design time because of the reduction of **timing** complexities.

**21/5/11 (Item 1 from file: 2)**
DIALOG(R)File 2:INSPEC


4818740 INSPEC Abstract Number: C9412-6150N-125
**Title: A database server for distributed real-time systems: issues and experiences**
Author(s): Young-Kuk Kim; Lehr, M.R.; George, D.W.; Son, S.H.
Author Affiliation: Dept. of Comput. Sci., Virginia Univ., Charlottesville, VA, USA
p.66-75
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1994 Country of Publication: USA x+213 pp.
ISBN: 0 8186 6420 7
U.S. Copyright Clearance Center Code: 0 8186 6420 7/94/$03.00
Conference Title: Second Workshop on Parallel and Distributed Real-Time Systems
Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Real-Time Syst.; IEEE Comput. Soc. Tech. Committee on Parallel Process
Conference Date: 28-29 April 1994 Conference Location: Cancun, Mexico
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: The design and implementation of database systems for real-time

applications presents many new and challenging problems. In addition to maintaining data consistency, the **database** system must satisfy **timing** constraints associated with transactions. In this paper we present our experiences in integrating a database server with a real-time operating system kernel and our attempts at providing flexible control for concurrent transaction management. We chose the ARTS operating system kernel as the basis for the real-time database server. Current research issues involving the development of a **programming interface** and imprecise computing server are also discussed. (19 Refs)

Subfile: C

Descriptors: data integrity; database management systems; distributed processing; network operating systems; operating systems (computers); real-time systems; scheduling

Identifiers: database server; distributed real-time systems; database systems; data consistency; timing constraints; real-time operating system kernel; concurrent transaction management; ARTS; **programming interface** ; imprecise computing server

Class Codes: C6150N (Distributed systems); C6160 (Database management systems (DBMS)); C6130S (Data security); C6150J (Operating systems)

**21/5/12 (Item 2 from file: 2)**



04121049 INSPEC Abstract Number: C9205-6160D-010

**Title: RTDB: a real-time database manager for time-critical applications**

Author(s): Sang H. Son; Iannacone, C.C.; Poris, M.S.

Author Affiliation: Dept. of Comput. Sci., Virginia Univ., Charlottesville, VA, USA

Conference Title: Proceedings. EUROMICRO '91. Workshop on Real-Time Systems p.207-14

Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA

Publication Date: 1991 Country of Publication: USA ix+231 pp.

ISBN: 0 8186 2210 5

U.S. Copyright Clearance Center Code: 0 8186 2212 1/91/0000/0207$01.00

Conference Sponsor: IEEE

Conference Date: 12-14 June 1991 Conference Location: Paris-Orsay, France

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: Compared with traditional databases, database systems for time-critical applications have the distinct feature that they must satisfy timing constraints associated with transactions. Transactions in real-time database systems should be scheduled considering both data consistency and **timing** constraints. Since a **database** system must operate in the context of available operating system services, an environment for database systems development must provide facilities to support operating system functions and integrate them with database systems for experimentation. The authors chose the ARTS real-time operating system kernel. They present their experience in integrating a relational database manager with a real-time operating system kernel, and their attempts at providing flexible control for concurrent transaction management. On-going research issues involving the development of a **programming interface** and the authors' efforts in using these techniques in implementing a specific experimental application (DOSE, distributed operating system experiment) are also discussed. (19 Refs)

Subfile: C

Descriptors: operating systems (computers); real-time systems; relational databases; transaction processing

Identifiers: DOSE; RTDB; real-time database manager; time-critical applications; timing constraints; data consistency; operating system services; database systems development; ARTS real-time operating system kernel; relational database manager; flexible control; concurrent transaction management; **programming interface** ; DOSE; distributed operating system experiment

Class Codes: C6160D (Relational DBMS); C6150J (Operating systems)

**21/5/13 (Item 3 from file: 2)**
DIALOG(R)File 2:INSPEC


03076979 INSPEC Abstract Number: B88015112, C88013263
**Title: Talking to the host (PC-to-mainframe connections)**
Author(s): Mack, R.
Author Affiliation: Deloitte Haskins & Sells, London, UK
Journal: Systems International vol.15, no.12 p.55-6, 58
Publication Date: Dec. 1987 Country of Publication: UK
CODEN: SYIND8 ISSN: 0309-1171
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The author describes PC-to-mainframe links and how they vary from simple **asynchronous** terminal emulators to RJE terminal emulators. The advent of LAN-based communication products, however, allows more efficient use of host communication ports. Such products include IBM's terminal cluster **controller** , SRPI (Server-Requester **Programming Interface** ), and ECF (Enhanced Connectivity Facilities). These and other such IBM products are discussed. Some of the issues facing management who may be implementing such links, are also considered. (0 Refs)
Subfile: B C
Descriptors: computer communications software; data communication equipment; DP management; inter-computer links; local area networks
Identifiers: remote job entry emulators; TRN; DP management; **synchronous** connection; personal computers; token ring network; PC-to-mainframe connections; **asynchronous** terminal emulators; RJE terminal emulators; LAN-based communication products; host communication ports; terminal cluster **controller** ; SRPI; Server-Requester **Programming Interface** ; ECF ; Enhanced Connectivity Facilities; IBM products
Class Codes: B6210L (Computer communications); C0310 (EDP management); C5620L (Local area networks); C5630 (Networking equipment); C5690 (Other data communication equipment and techniques); C6155 (Computer communications software)

**21/5/14 (Item 4 from file: 2)**
DIALOG(R)File 2:INSPEC


01878631 INSPEC Abstract Number: B82034925, C82027059
**Title: Verification logic for telecommunication adapter automatic functions**
Author(s): Benignus, D.M.; Parker, T.S.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.24, no.9 p.4569-70
Publication Date: Feb. 1982 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P)
Abstract: Describes a technique for the verification of automatic functions of a telecommunication adapter which uses standard integrated circuit modules on a common card. (0 Refs)
Subfile: B C
Descriptors: data communication equipment; integrated circuit testing; logic testing
Identifiers: verification logic; **programmable** communication **interface** ; universal **synchronous / asynchronous** receive/transmit circuit; protocol **controller** ; OR gate; AND gate; telecommunication adapter automatic functions
Class Codes: B1265B (Logic circuits); C5210 (Logic design methods); C5600 (Data communication equipment and techniques)

**21/5/15 (Item 5 from file: 2)**
DIALOG(R)File 2:INSPEC

01474214 INSPEC Abstract Number: B80010888, C80008926
**Title:** Programmable **communications** interface **for popular microprocessors**
Journal: Australian Electronics Engineering vol.12, no.6 p.14, 16, 18-19, 22-3
Publication Date: June 1979 Country of Publication: Australia
CODEN: AUEEB5 ISSN: 0004-9042
Language: English Document Type: Journal Paper (JP)
Treatment: Economic aspects (E); Practical (P)
Abstract: The Signetics 2651 **Programmable** Communications **Interface** (PCI) is a universal **synchronous** / **asynchronous** data communications **controller** chip designed for microcomputer systems. The 2651 accepts programmed instructions from a microprocessor and supports many serial data communication disciplines, **synchronous** and **asynchronous** in the full or half-duplex mode. Although designed primarily for use with a 2650 microprocessor, the 2651 can be easily integrated into systems employing other CPUs. This article describes the use of the PCI with 8080A, 8085, SC/MP, Z80, 6800, and 8048-based systems. (0 Refs)
Subfile: B C
Descriptors: computer interfaces; microprocessor chips
Identifiers: **Programmable** Communications **Interface** ; data communications **controller** chip; microcomputer systems
Class Codes: B6210L (Computer communications); C5130 (Microprocessor chips); C5610 (Computer interfaces)

**21/5/16 (Item 6 from file: 2)**
DIALOG(R)File 2:INSPEC


00694392 INSPEC Abstract Number: B74037022, C74023281
**Title: Multiplexing (in The Dataroute)**
Author(s): Keyes, N.T.; Mueller, D.J.
Author Affiliation: Computer Transmission Corp., El Segundo, CA, USA
Conference Title: International Conference on Communications p.2B/1-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1974 Country of Publication: USA xxi+912 pp.
Conference Sponsor: IEEE
Conference Date: 17-19 June 1974 Conference Location: Minneapolis, MN, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Describes the **synchronous** and **asynchronous** time division multiplexers used in The Dataroute. They were designed to be part of a large, digital, master- **clocked** , **synchronous** network. Network requirements such as circuit routing flexibility, minimum propagation delays, network management and maintainability are discussed. The central theme of the design has been to include network alarm and diagnostic capability sufficient to allow **end** -to- **end** circuit testing, not only from serving **end** offices, but also from midpoint offices and regional test centers. The basic operational features of the multiplexers are reviewed in relation to the requirements. The **clocking** , framing, data rate **programming** and **interface** sections are discussed. (0 Refs)
Subfile: B C
Descriptors: data communication equipment; multiplexing equipment; time division multiplexing
Identifiers: Dataroute; time division multiplexers; **synchronous** network ; circuit routeing flexibility; minimum propagation delays; network management; maintainability; diagnostic capability; **clocking** ; framing; data rate programming; interface sections
Class Codes: B6210Z (Other data transmission); C5620 (Computer networks and techniques)

**21/5/17 (Item 1 from file: 233)**
DIALOG(R)File 233:Internet & Personal Comp. Abs.

00581178 00SU03-002
**Want to maintain Windows 2000 at peak performance? Defragment**
Robb, Drew
Storage Management Solutions , March 1, 2000 , v5 n2 p8-10, 3 Page(s)
ISSN: 1097-5152
Company Name: Microsoft
Product Name: Microsoft Windows 2000
Languages: English
Document Type: Articles, News & Columns
Geographic Location: United States
Examines the importance of defragmentation in Microsoft Windows 2000 operating system. Discusses file system changes in Windows 2000 that relate to defragmentation, namely enlargement of the reserved disk space called MFT Zone that allows for Master File Table (MFT) growth, a feature called Hibernate File where memory data is deposited during hibernation, and enhancement of the **application programming interfaces** (APIs) to support online defragmentation of directories. Describes the functionality and limitations of Windows 2000's built-in manual defragmenter utility, such as lack of scheduling, requirement for administrator privileges to operate, and inability to run several partitions concurrently. Presents tips for keeping Windows 2000 running at peak performance, such as obtaining defragmentation software at the time of Windows 2000 purchase and conducting defragmentation at regular **intervals** . Includes a **table** and a photo. (MEM)
Descriptors: Optimization; Hard Disk Drive; Operating Systems; File Management; Enterprise Computing; Maintenance
Identifiers: Microsoft Windows 2000; Microsoft

**21/5/18 (Item 2 from file: 233)**
DIALOG(R)File 233:Internet & Personal Comp. Abs.


00174934 88PK08-211
**Intel spec expected to support** synchronous **links**
Kramer, Matt
PC Week , August 15, 1988 , v5 n33 p5, 1 Pages
ISSN: 0740-1604
Languages: English
Document Type: Feature Articles and News
Geographic Location: United States
Reports that Intel Corp.'s Intel Communications Applications Specification (ICAS) is expected to support **synchronous** communication, in addition to **asynchronous** and facsimile communication. A source familiar with ICAS indicates that it is a higher level specification than IBM's High-Level Language **Applications Program Interface** (HLLAPI) and differs from it in that ICAS **controls timing** and other mechanics of communications thro transfer agents, freeing the developer from these concerns. Contains one diagram. (djd)
Descriptors: Data Communication
Identifiers: ICAS; Intel

**21/5/19 (Item 1 from file: 144)**
DIALOG(R)File 144:Pascal


14182098 PASCAL No.: 99-0380830
**Conception de systemes embarques : Codesign d'un controleur de protocole aeronautique**
**Colloque CAO de circuits integres et systemes : Aix en Provence, 10-12 mai 1999**
**(Embedded systems design : Codesign of aeronautic protocol** controller **)**
CLOUTE F; CONTENSOU J N; ESTEVE D; PAMPAGNIN P; PONS P; FAVARD Y
Laboratoire d'Electronique LEN7 de l'ENSEEIHT, Groupe Conception Electronique, 2, rue Charles Camichel, 31071 Toulouse, France; AEROSPATIALE-Branche Aeronautique, Direction Systemes et Services, 316,

route de Bayonne, 31060 Toulouse, France
CNRS. CAO de circuits et de systemes electroniques, Grenoble, France.
Colloque CAO de circuits integres et systemes (Aix en Provence FRA)
1999-05-10
1999 68-71
ISBN: 2-913329-20-9 Availability: INIST-Y 32278; 354000084546300150
No. of Refs.: 11 ref.
Document Type: C (Conference Proceedings) ; A (Analytic)
Country of Publication: France
Language: French
Avec la complexite croissante des systemes numeriques, leur conception aboutit a de reels problemes d'integration du materiel et du logiciel lors du prototypage physique. Une methodologie de CAO de codesign materiel/logiciel devient indispensable. Cette methodologie repose sur une (co)specification executable au niveau systeme independante de l'implementation, qui permette d'evaluer differentes architectures, avant la synthese automatique de l'architecture heterogene retenue. Cet article presente une **application** aeronautique: une **interface** du protocole ARINC de communication. L'approche de codesign est basee sur l'environnement POLIS/Ptolemy. Le systeme distribue est specifie par un modele de communication **asynchrone** entre des modules definis avec le langage **synchrone** Esterel. L'architecture cible est constituee d'un microcontroleur et d'un ou plusieurs coprocesseurs dedies.

English Descriptors: System design; Computer aided design; Software tool; Methodology; Transmission protocol; Aeronautic industry; Distributed system; **Asynchronous** transmission; System synthesis; Microprocessor; **Controller** ; Embedded system; Codesign

French Descriptors: Conception systeme; Conception assistee; Outil logiciel ; Methodologie; Protocole transmission; Industrie aeronautique; Systeme reparti; Transmission **asynchrone** ; Synthese systeme; Microprocesseur; Controleur; Esterel; ARINC; POLIS/Ptolemy; Systeme embarque; Codesign

Classification Codes: 001D03F06A



**21/5/20 (Item 2 from file: 144)**
DIALOG(R)File 144:Pascal


12353820 PASCAL No.: 95-0599375
**Applications of fibre optic networks in high technology research**
MURPHY BAKES C; GOLDBERG F N
Kent State Univ, Kent OH, USA
Journal: International Journal of Computer Applications in Technology, 1995, 8 (3-4) 172-189
ISSN: 0952-8091 CODEN: IJCTEK Availability: E.i.
No. of Refs.: 25 Refs.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: United Kingdom
Language: English
The NASA Lewis Research Center has active programmes in fluid dynamics and solid dynamics. These require a communications network capable of transporting multimedia traffic, including data, voice, interactive and non-interactive video, real-time visualization, and data gathering from scientific experiments. The use of powerful desktop workstations, which operate as standalone devices, work cooperatively in local clusters, operate in client server mode, access central computers, and address remote sites, also impacts on network requirements. This paper provides an overview of FDDI and SONET networks and investigates their roles in supporting high-level technological research FDDI's topology, reliability, traffic classes, data encoding, token ring operation, **timers** , network **management** issues, and candidate applications are discussed. The multiplexing hierarchy, optical signal format, OAM capability, survivability, and candidate applications of SONET networks are explored.

Interoperability issues, with the SDH international standard, ATM packet switching, and BISDN networks, are also addressed.

English Descriptors: High technology research; Multiplexing hierarchy; Fibre distributed data interface; **Synchronous** optical network; Optical signal format; Survivability; **Application** ; User **interfaces** ; Computer networks; Research; Electric network topology; Reliability; Telecommunication traffic; Signal encoding; Local area networks; Multiplexing; Standards; **Asynchronous** transfer mode; Broadband networks ; Fiber optic networks

French Descriptors: **Application** ; **Interface utilisateur** ; Reseau ordinateur; Recherche; Topologie reseau electrique; Fiabilite; Teletrafic ; Codage signal; Reseau local; Multiplexage; Norme; Transmission **asynchrone** ; Reseau large bande; Reseau fibre optique

Classification Codes: 001D04B02G; 001D03J03; 001D03J; 001D00E; 001D00C

**21/5/21 (Item 1 from file: 34)**
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci


03227296 Genuine Article#: NP066 Number of References: 15
**Title: ZEB - SOFTWARE FOR INTEGRATION, DISPLAY, AND MANAGEMENT OF DIVERSE ENVIRONMENTAL DATASETS**
Author(s): CORBET J; MUELLER C; BURGHART C; GOULD K; GRANGER G
Corporate Source: NCAR,DIV ATMOSPHER TECHNOL,SURFACE & SOUNDING SYST FACIL,POB 3000/BOULDER//CO/80307; NCAR,DIV ATMOSPHER TECHNOL,SURFACE & SOUNDING SYST FACIL,POB 3000/BOULDER//CO/80307
Journal: BULLETIN OF THE AMERICAN METEOROLOGICAL SOCIETY, 1994, V75, N5 ( MAY), P783-792
ISSN: 0003-0007
Language: ENGLISH Document Type: ARTICLE
Geographic Location: USA
Subfile: SciSearch; CC PHYS--Current Contents, Physical, Chemical & Earth Sciences
Journal Subject Category: METEOROLOGY & ATMOSPHERIC SCIENCES
Abstract: This paper describes the Zeb software for integration, display, and management of diverse environmental datasets. Zeb's primary use is for the superpositioning of observational datasets (such as those collected by satellite, radar, mesonet, and aircraft) and analysis products (such as model results, dual-Doppler synthesis, or algorithm output). Data may be overlaid on a variety of display types, including constant altitude planes, vertical cross sections, X-Y graphs, skew T plots, and time-height profiles. The fields for display, color **tables** , contour **intervals** , and various other display options are defined using an icon-based user interface. This highly flexible system allows scientific investigators to interactively superimpose and highlight diverse datasets, thus aiding data interpretation.

Data handling capabilities permit external analysis programs to be easily linked with display and data storage processes. The data store accepts incoming data, stores it on disk, and makes it available to processes that need it. An application library is available for data handling. The library functions allow data storage, retrieval, and queries using a single **applications interface** , regardless of the data's source and organization.

The software system runs under Unix and the X Window system. Zeb has been used for real-time project control as well as data interpretation at investigators' home institutions. Features and implementation are explained along with examples of graphic output.
Cited References:
ASENTE PJ, 1990, X WINDOW SYSTEM TOOL
BROCK FV, 1981, P700, 20TH C RAD MET BOST
BURGHART C, 1989, P573, 24TH C RAD MET TALL

DIRKS RA, 1988, V69, P148, B AM METEOROL SOC
DOSWELL CA, 1986, P177, 11TH P C WEA FOR AN
GOULD JD, 1985, V3, P300, COMMUN ACM
HAYDEN G, 1980, REQUIREMENTS ANAL EV
HORTON G, 1992, WINDOW DISPLAY SYSTE
MILLER LJ, 1993, CEDRIC CUSTOM EDITIN
MOORE JA, 1989, P605, 24TH C RAD MET TALL
OUSTERHOUT J, 1993, INTRO TCL TK
POSTEL JB, 1980, USER DATAGRAM PROTOC
REW R, 1990, V10, P76, IEEE COMPUT GRAPH
SCHEIFLER RW, 1986, V2, P79, ACM T GRAPHIC
SCHNEIDERMAN B, 1983, V16, P57, IEEE COMPUT

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Set     Items   Description
S1         17   AU=(DAMON P? OR DAMON, P)
S2         85   AU=(HEDDES M? OR HEDDES, M?)
S3          5   S1 AND S2
S4         35   (S1 OR S2) AND IC=(G06F-015? OR G06F-009?)
S5         37   S3 OR S4
S6         37   IDPAT (sorted in duplicate/non-duplicate order)
S7         23   IDPAT (primary/non-duplicate records only)
File 344:Chinese Patents Abs Aug 1985-2003/Jan
         (c) 2003 European Patent Office
File 347:JAPIO Oct 1976-2002/Dec(Updated 030402)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200323
         (c) 2003  Thomson Derwent
File 348:EUROPEAN PATENTS 1978-2003/Mar W05
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030403,UT=20030327
         (c) 2003 WIPO/Univentio
```

**7/5/1 (Item 1 from file: 350)**



015159103 **Image available**
WPI Acc No: 2003-219631/200321
XRPX Acc No: N03-175094

**Frame transmission completion determination method for network processors, involves supplying state of last bit of control information to transmission system of network processor**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: BASSO C; CALVIGNAC J L; **HEDDES M C** ; LOGAN J F; VERPLANKEN F J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020147830 | A1 | 20021010 | US 2001828342 | A | 20010406 | 200321 | B |

Priority Applications (No Type Date): US 2001828342 A 20010406
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020147830 | A1 | | 9 | G06F-015/16 | |

Abstract (Basic): US 20020147830 A1

NOVELTY - Several buffer blocks with space for storing control information to link one buffer to another, are provided. The buffer control flag has last bit flag bit which assumes either zero or one, based on the necessity to chain additional buffer to previous buffer. The state of the last bit of control information is supplied to the transmission system of network processor.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for buffer control blocks.

USE - For determining completion of frame transmission by network processor.

ADVANTAGE - Conveniently determines the end of frame transmission using the information contained in buffer control block.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the frame transmission completion.

pp; 9 DwgNo 5/5

Title Terms: FRAME; TRANSMISSION; COMPLETE; DETERMINE; METHOD; NETWORK; PROCESSOR; SUPPLY; STATE; LAST; BIT; CONTROL; INFORMATION; TRANSMISSION; SYSTEM; NETWORK; PROCESSOR
Derwent Class: W01
International Patent Class (Main): **G06F-015/16**
File Segment: EPI

**7/5/2 (Item 2 from file: 350)**



015042311 **Image available**
WPI Acc No: 2003-102827/200309
XRPX Acc No: N03-082163

**IP fragmentation method for network processor, involves storing IP frames fragments in buffers which are returned to free buffer queue, when all fragments are transmitted to network processor**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: BASSO C; CALVIGNAC J L; **HEDDES M C** ; LOGAN J F; VERPLANKEN F J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020156908 | A1 | 20021024 | US 2001839010 | A | 20010420 | 200309 | B |

Priority Applications (No Type Date): US 2001839010 A 20010420
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020156908 | A1 | | 18 | G06F-015/16 | |

Abstract (Basic): US 20020156908 A1

NOVELTY - Initially a series of buffers (1011-1015) are placed in a free buffer queue. When an Internet protocol (IP) frame to be fragmented is received, the buffers are popped from the queue to store the frame fragments to be dispatched to the network processor. When all the frame fragments are transmitted to the processor, the buffers are returned to the buffer queue.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for network processor.

USE - For fragmenting Internet protocol (LP) frame ON network processor (claimed) in telecommunication network.

ADVANTAGE - The frame fragments are stored in a series of buffers which are returned to a free buffer queue when all the fragments are transmitted to the network processor. Therefore the need to copy the entire frame for each multi cast instance is eliminated, thereby reducing the memory requirements and solving the problems due to post performance discrepancies.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the IP fragmentation system.

Buffers (1011-1015)

pp; 18 DwgNo 1/7

Title Terms: IP; FRAGMENT; METHOD; NETWORK; PROCESSOR; STORAGE; IP; FRAME; FRAGMENT; BUFFER; RETURN; FREE; BUFFER; QUEUE; FRAGMENT; TRANSMIT; NETWORK; PROCESSOR

Derwent Class: T01; W01

International Patent Class (Main): **G06F-015/16**

File Segment: EPI

**7/5/3 (Item 3 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



014968238 **Image available**

WPI Acc No: 2003-028752/200302

XRPX Acc No: N03-022604

**Network device has interconnected network processor complex chip, data flow chip and scheduler chip, each having separate memory**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); CIE IBM FRANCE (IBMC )

Inventor: CALVIGNAC J L; GOETZINGER W J; HANDLOGTEN G H; **HEDDES M C ;** LOGAN J F; MIKOS J F; NORGAARD D A; VERPLANKEN F J; VERPLANKEN F

Number of Countries: 100 Number of Patents: 002

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020122386 | A1 | 20020905 | US 2001273438 | A | 20010305 | 200302 | B |
| | | | US 2001838395 | A | 20010419 | | |
| WO 200271206 | A2 | 20020912 | WO 2002EP1955 | A | 20020131 | 200302 | |

Priority Applications (No Type Date): US 2001273438 P 20010305; US 2001838395 A 20010419

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020122386 | A1 | | 14 | H04J-003/14 | Provisional application US 2001273438 |
| WO 200271206 | A2 | E | | G06F-009/00 | |

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 20020122386 A1

NOVELTY - A network processor complex chip executes programs to forward frames or hardware assist functions to perform operations like table searches, policing and counting. A data flow chip

receives/transmits data, and sets its ports into switch mode and/or line mode. A scheduler chip schedules frames to meet predetermined quality of service commitments. Each of these interconnected chips has separate memories.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for network processor.

USE - For processing frames or packets in communications network.

ADVANTAGE - Processes data packets at a higher rate.

DESCRIPTION OF DRAWING(S) - The figure shows a network device having a network processor.

pp; 14 DwgNo 2/5

Title Terms: NETWORK; DEVICE; INTERCONNECT; NETWORK; PROCESSOR; COMPLEX; CHIP; DATA; FLOW; CHIP; CHIP; SEPARATE; MEMORY

Derwent Class: T01; W01

International Patent Class (Main): **G06F-009/00** ; H04J-003/14

File Segment: EPI

**7/5/4 (Item 4 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



014584385 **Image available**

WPI Acc No: 2002-405089/200243

XRPX Acc No: N02-318002

**Timer management system for data processing system, has timer services with handle function to output time-out message to user application or to application's task, on timer expiration**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); IBM UK LTD (IBMC )

Inventor: **DAMON P** ; **HEDDES M**

Number of Countries: 096 Number of Patents: 002

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200227468 | A2 | 20020404 | WO 2001GB4322 | A | 20010927 | 200243 | B |
| AU 200190129 | A | 20020408 | AU 200190129 | A | 20010927 | 200252 | |

Priority Applications (No Type Date): US 2000675545 A 20000928

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200227468 | A2 | E | 24 | G06F-009/00 | |

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

| | | | | |
|---|---|---|---|---|
| AU 200190129 | A | | G06F-009/00 | Based on patent WO 200227468 |

Abstract (Basic): WO 200227468 A2

NOVELTY - An API (220) provides a set of synchronous functions that allows the user applications (210) to access timer database (230). Timer services (240) detects expiration of timers corresponding to each application that has initiated the timer via API, which has handle function to output a time-out message to user application or to application's task, on expiration, based on the type of utilized system, without incurring an illegal time-out messages.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Timer management method in both synchronous and asynchronous system;

(b) Computer program for controlling data processing operation

USE - For managing timers in both synchronous and asynchronous data processing system.

ADVANTAGE - The handle function filters the illegal time-out messages by allowing the asynchronous application to synchronously act on the timer in the asynchronous system. The timer services detects the expiring of the timers in order to manage both single task system and multi-task system.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of a timer management system.
User application (210)
API (220)
Timer database (230)
Timer service (240)
pp; 24 DwgNo 2/4
Title Terms: TIME; MANAGEMENT; SYSTEM; DATA; PROCESS; SYSTEM; TIME; SERVICE ; HANDLE; FUNCTION; OUTPUT; TIME; MESSAGE; USER; APPLY; APPLY; TASK; TIME ; EXPIRE
Derwent Class: T01
International Patent Class (Main): **G06F-009/00**
File Segment: EPI

**7/5/5 (Item 5 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014533721 **Image available**
WPI Acc No: 2002-354424/200239
XRPX Acc No: N02-278540
**Program instruction processing system for use with network computer system, has interface enabling mapping of special purpose registers of main processing unit and co-processor, into common address map**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: DAVIS G T; **HEDDES M C** ; LEAVENS R B; RINALDI M A
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| GB 2366426 | A | 20020306 | GB 20018828 | A | 20010409 | 200239 | B |

Priority Applications (No Type Date): US 2000548109 A 20000412
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| GB 2366426 | A | | 27 | G06F-009/38 | |

Abstract (Basic): GB 2366426 A
NOVELTY - An interface between a main processing unit and a co-processor, enables configuration of the co-processor unit, and initiation of the specific tasks to be completed by the co-processor unit. Status information corresponding to the co-processor unit is accessed and the task results are returned. The interface enables mapping of the special purpose registers of the main processing unit and the co-processor, into a common address map.
USE - For processing program instructions in network computer system.
ADVANTAGE - Coprocessors provide hardware acceleration for specific network processing tasks like high speed pattern search, data manipulation, internal chip management functions frame paving and data fetching.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of a protocol processing unit of the processing system.
pp; 27 DwgNo 1/9
Title Terms: PROGRAM; INSTRUCTION; PROCESS; SYSTEM; NETWORK; COMPUTER; SYSTEM; INTERFACE; ENABLE; MAP; SPECIAL; PURPOSE; REGISTER; MAIN; PROCESS ; UNIT; CO; PROCESSOR; COMMON; ADDRESS; MAP
Derwent Class: T01
International Patent Class (Main): **G06F-009/38**
International Patent Class (Additional): **G06F-015/16** ; **G06F-015/17**
File Segment: EPI

**7/5/6 (Item 6 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014530181 **Image available**

WPI Acc No: 2002-350884/200238
XRPX Acc No: N02-275692

**Frame processing and enqueuing system for communication network apparatus, removes frames from calender, when user selected type of service exceeds bandwidth limit set for the service, according to stored logic**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: BASS B M; CALVIGNAC J L; **HEDDES M C** ; SIEGEL M S; VERPLANKEN F J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020023168 | A1 | 20020221 | US 2000196831 | P | 20000413 | 200238 | B |
| | | | US 2001834141 | A | 20010412 | | |

Priority Applications (No Type Date): US 2000196831 P 20000413; US 2001834141 A 20010412
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020023168 | A1 | | 23 | G06F-015/16 | Provisional application US 2000196831 |

Abstract (Basic): US 20020023168 A1

NOVELTY - Frames are placed in corresponding calender (220,230,250) based on type of service selected by users. When the user selected type of service exceeds bandwidth limit set for the service, the frames are removed from the calenders in accordance with stored logic.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for processed frames placement method.

USE - For communication network apparatus.

ADVANTAGE - Allows usage of unused bandwidth by other users through the use of weighted fair queuing system at any time, thereby improves efficiency of the system. Provides different levels of service by establishing different calenders.

DESCRIPTION OF DRAWING(S) - The figure shows Egress scheduler of frame processing and enqueuing system.

Calenders (220,230,250)

pp; 23 DwgNo 3/13

Title Terms: FRAME; PROCESS; SYSTEM; COMMUNICATE; NETWORK; APPARATUS; REMOVE; FRAME; CALENDER; USER; SELECT; TYPE; SERVICE; BANDWIDTH; LIMIT; SET; SERVICE; ACCORD; STORAGE; LOGIC
Derwent Class: T01; W01
International Patent Class (Main): **G06F-015/16**
File Segment: EPI

**7/5/7 (Item 7 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014405878 **Image available**
WPI Acc No: 2002-226581/200228
XRPX Acc No: N02-173930

**Information distribution scheduler for information handling system in network, generates signal to transfer single information packet or frame, selected based on stored rules, towards destination**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); IBM UK LTD (IBMC )
Inventor: BASS B M; CALVIGNAC J L; **HEDDES M** ; SIEGEL M S; VERPLANKEN F J
Number of Countries: 094 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200179992 | A2 | 20011025 | WO 2001GB1337 | A | 20010326 | 200228 | B |
| AU 200144309 | A | 20011030 | AU 200144309 | A | 20010326 | 200228 | |
| EP 1273140 | A2 | 20030108 | EP 2001917224 | A | 20010326 | 200311 | |
| | | | WO 2001GB1337 | A | 20010326 | | |

Priority Applications (No Type Date): US 2000548913 A 20000413; US 2000548910 A 20000413; US 2000548912 A 20000413
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200179992 | A2 | E | 42 | G06F-009/00 | |

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
AU 200144309 A G06F-009/00 Based on patent WO 200179992
EP 1273140 A2 E H04L-012/56 Based on patent WO 200179992
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): WO 200179992 A2
NOVELTY - Time based and time independent calendars handle respective information packets/frames passing in a data communication system, from different sources to different destinations based on prestored source related information. A timer periodically generates a signal to transfer a single information packet or frame, which is selected based on stored rules, towards the corresponding destination.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for information distribution scheduling method.
USE - For information handling systems or computers in communication networks e.g. Internet, intranet and for DN enqueue system and scheduler.
ADVANTAGE - Allows efficient use of bandwidth resource and allows service level commitments to be fulfilled while allowing any other remaining bandwidth to be used efficiently and equitably. Packets of different lengths can be handled.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of interface device with embedded processor complex.
pp; 42 DwgNo 1/15
Title Terms: INFORMATION; DISTRIBUTE; INFORMATION; HANDLE; SYSTEM; NETWORK; GENERATE; SIGNAL; TRANSFER; SINGLE; INFORMATION; PACKET; FRAME; SELECT; BASED; STORAGE; RULE; DESTINATION
Derwent Class: T01; W01
International Patent Class (Main): **G06F-009/00** ; H04L-012/56
International Patent Class (Additional): H04Q-011/04
File Segment: EPI

**7/5/8 (Item 8 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014293115 **Image available**
WPI Acc No: 2002-113817/200215
Related WPI Acc No: 2001-235135; 2001-273355; 2001-281404; 2001-589548; 2001-625628
XRPX Acc No: N02-084875
**Memory system in computers, includes controller which provides access simultaneously to all or some of storage modules in response to multiple request from multiple sources**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); BASS B M (BASS-I); HEDDES M C (HEDD-I); PATEL P C (PATE-I); REVILLA J G (REVI-I); SIEGEL M S (SIEG-I); VERPLANKEN F J (VERP-I)
Inventor: BASS B M; CALVIGNAC J L; **HEDDES M C** ; PATEL P C; REVILLA J G; SIEGEL M S; VERPLANKEN F J
Number of Countries: 024 Number of Patents: 007
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200116779 | A1 | 20010308 | WO 2000US20794 | A | 20000824 | 200215 | B |
| EP 1208447 | A1 | 20020529 | EP 2000959157 | A | 20000824 | 200243 | |
| | | | WO 2000US20794 | A | 20000824 | | |
| US 20020099855 | A1 | 20020725 | US 99384744 | A | 19990827 | 200254 | |
| KR 2002024332 | A | 20020329 | KR 2002702332 | A | 20020222 | 200265 | |
| US 6460120 | B1 | 20021001 | US 99384744 | A | 19990827 | 200268 | |
| CN 1369074 | A | 20020911 | CN 2000811557 | A | 20000824 | 200282 | |
| JP 2003508851 | W | 20030304 | WO 2000US20794 | A | 20000824 | 200319 | |
| | | | JP 2001520663 | A | 20000824 | | |

Priority Applications (No Type Date): US 99384744 A 19990827
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 200116779 A1 E 79 G06F-015/16
Designated States (National): CN JP KR SG
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
EP 1208447 A1 E G06F-015/16 Based on patent WO 200116779
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
US 20020099855 A1 G06F-015/16
KR 2002024332 A G06F-013/00
US 6460120 B1 G06F-013/00
CN 1369074 A G06F-015/16
JP 2003508851 W 89 G06F-012/06 Based on patent WO 200116779

Abstract (Basic): WO 200116779 A1
NOVELTY - The memory controller comprising tree search memory arbiter (TSM), control devices and bus structure is connected to storage modules including SRAMs and DRAMs. The memory controller in response to multiple request from multiple sources provides access simultaneously to all or some of storage modules.
DETAILED DESCRIPTION - The multiple request are received simultaneously. Several embedded processors (GasteriskH) are coupled to memory controller and the multiple request are generated. The arbiters (TSM) are respectively coupled to one storage module and controlling access to one storage module. The control devices are coupled to processors (GasteriskH) to generate storage request signals indicating access to one of the storage modules. The bus structure is coupled to control devices and arbiters so that control device has access to all or some of storage modules. An INDEPENDENT CLAIM is also included for method for operating network switch apparatus.
USE - In computers.
ADVANTAGE - The SRAM arbiter efficiently manages the flow of data between the embedded processor and ON chip and OFF chip SRAMs. The DRAM arbiter efficiently manages the flow of data between embedded processor and OFF chip DRAM devices.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of memory complex.
pp; 79 DwgNo 13/18
Title Terms: MEMORY; SYSTEM; COMPUTER; CONTROL; ACCESS; SIMULTANEOUS; STORAGE; MODULE; RESPOND; MULTIPLE; REQUEST; MULTIPLE; SOURCE
Derwent Class: T01; U14
International Patent Class (Main): G06F-012/06; G06F-013/00; **G06F-015/16**
International Patent Class (Additional): G06F-012/00; **G06F-015/167** ; **G06F-015/177** ; H04L-012/28; H04L-012/56
File Segment: EPI

**7/5/9 (Item 9 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014247668
WPI Acc No: 2002-068368/200210
XRPX Acc No: N02-050630
**Network processor architecture has control message formatting service that converts OS or hardware specific request into general request applicable to any OS or hardware and vice-versa**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); IBM CORP (IBMC )
Inventor: BASSO C; **DAMON P** ; GALLO A M
Number of Countries: 028 Number of Patents: 003
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
EP 1161045 A2 20011205 EP 200157 A 20010316 200210 B
JP 2001325203 A 20011122 JP 200192526 A 20010328 200210
KR 2001091013 A 20011022 KR 200112156 A 20010309 200221

Priority Applications (No Type Date): US 2000546133 A 20000410
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
EP 1161045    A2 E  12 H04L-029/06
   Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
JP 2001325203 A     12 G06F-013/10
KR 2001091013 A        G06F-015/00

Abstract (Basic): EP 1161045 A2
NOVELTY - A control message formatting service that operates as an interpreter within a device drive converts all low and high level APIs or various components into a specific language used by a network processor. The control message formatting service converts an operating system (OS) or hardware specific request into a general request applicable to any OS or hardware and vice-versa.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) a computer program product;
(b) a control system;
(c) and a device driver program.
USE - For computer system.
ADVANTAGE - Provides additional functional utilities based on customer needs of network develop design. Solves problem of determining how to manage network interfaces and how to decompose and fit services into system with existing and new interfaces by providing unique device drive mechanism for managing network processor.
pp; 12 DwgNo 0/3
Title Terms: NETWORK; PROCESSOR; ARCHITECTURE; CONTROL; MESSAGE; FORMAT; SERVICE; CONVERT; OS; HARDWARE; SPECIFIC; REQUEST; GENERAL; REQUEST; APPLY; OS; HARDWARE; VICE-VERSA
Derwent Class: W01
International Patent Class (Main): G06F-013/10; **G06F-015/00** ; H04L-029/06
International Patent Class (Additional): H04L-012/56
File Segment: EPI

**7/5/10 (Item 10 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014179888 **Image available**
WPI Acc No: 2002-000585/200201
XRPX Acc No: N02-000391
**Use of threads in connection with processor and accessible data by transferring execution control to next thread in queue if first thread is blocked**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); IBM CORP (IBMC )
Inventor: DAVIS G T; **HEDDES M C** ; LEAVENS R B; VERPLANKEN F J
Number of Countries: 004 Number of Patents: 004
Patent Family:
Patent No  Kind  Date  Applicat No  Kind  Date  Week
DE 10110504  A1  20011018  DE 1010504  A  20010303  200201  B
CA 2334393  A1  20011004  CA 2334393  A  20010202  200201
JP 2001350638  A  20011221  JP 2001104520  A  20010403  200206
KR 2001094951  A  20011103  KR 200111116  A  20010305  200223

Priority Applications (No Type Date): US 2000542206 A 20000404
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
DE 10110504   A1    11 G06F-009/46
CA 2334393    A1 E     G06F-009/38
JP 2001350638 A     14 G06F-009/46
KR 2001094951 A        G06F-015/16

Abstract (Basic): DE 10110504 A1
NOVELTY - The method involves providing several instruction

execution threads as independent processes in a sequential time frame. The execution threads are arranged in a queue so that they have overlapping access to the accessible data. A first thread in the queue is executed, and the execution control is transferred to the next thread in the queue when an event occurs that blocks the execution of the first thread.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for a processing system, a method of executing several independent threads in a processor, the use of a prefetch buffers in connection with a number of independent instruction threads, and for a thread execution controller.

USE - For computer systems in which the computer executes multiple instruction threads.

ADVANTAGE - Minimizes the effect of latency when accessing data formatted in a tree structure.

DESCRIPTION OF DRAWING(S) - The drawing shows a network processor architecture with two coprocessors.

pp; 11 DwgNo 1/4

Title Terms: THREAD; CONNECT; PROCESSOR; ACCESS; DATA; TRANSFER; EXECUTE; CONTROL; THREAD; QUEUE; FIRST; THREAD; BLOCK

Derwent Class: T01

International Patent Class (Main): **G06F-009/38 ; G06F-009/46 ; G06F-015/16**

International Patent Class (Additional): **G06F-009/48**

File Segment: EPI

**7/5/11 (Item 11 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



014126781 **Image available**

WPI Acc No: 2001-610991/200170

XRPX Acc No: N01-456118

**Controlling flow of several packets in computer network e.g. in ATM or Ethernet networks**

Patent Assignee: IBM UK LTD (IBMC ); INT BUSINESS MACHINES CORP (IBMC )

Inventor: AYDEMIR M; BASS B M; GALLO A M; GORTI B K; **HEDDES M** ; JEFFRIES C D; ROVNER S K; SIEGEL M S

Number of Countries: 094 Number of Patents: 005

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200139467 | A1 | 20010531 | WO 2000GB4410 | A | 20001121 | 200170 | B |
| AU 200114069 | A | 20010604 | AU 200114069 | A | 20001121 | 200170 | |
| EP 1232627 | A1 | 20020821 | EP 2000976194 | A | 20001121 | 200262 | |
| | | | WO 2000GB4410 | A | 20001121 | | |
| CZ 200201780 | A3 | 20021016 | WO 2000GB4410 | A | 20001121 | 200279 | |
| | | | CZ 20021780 | A | 20001121 | | |
| KR 2002063578 | A | 20020803 | KR 2002706623 | A | 20020523 | 200308 | |

Priority Applications (No Type Date): US 2000547280 A 20000411; US 99448190 A 19991123; US 99448197 A 19991123; US 99448380 A 19991123

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200139467 | A1 | E | 99 | H04L-029/06 | |
| Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW | | | | | |
| Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW | | | | | |
| AU 200114069 | A | | | H04L-029/06 | Based on patent WO 200139467 |
| EP 1232627 | A1 | E | | H04L-029/06 | Based on patent WO 200139467 |
| Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR | | | | | |
| CZ 200201780 | A3 | | | H04L-029/06 | Based on patent WO 200139467 |
| KR 2002063578 | A | | | H04L-012/56 | |

Abstract (Basic): WO 200139467 A1

NOVELTY - The computer network includes a device defining a queue. A queue level for the queue and an offered rate of the number of packets to the queue are determined. A transmission fraction of the number of packets to or from the queue is controlled based on the queue level; the offered rate and a previous value of the transmission fraction.

DETAILED DESCRIPTION - Hence the transmission fraction and the queue level are critically damped if the queue level is between at a first queue level and a second queue level.

USE - To control flow of several packets in computer network e.g. in ATM or Ethernet networks.

ADVANTAGE - Better and more effective control of traffic through a switch.

DESCRIPTION OF DRAWING(S) - The drawing shows a flow diagram of the method.

pp; 99 DwgNo 4/21

Title Terms: CONTROL; FLOW; PACKET; COMPUTER; NETWORK; ATM; NETWORK
Derwent Class: T01; W01
International Patent Class (Main): H04L-012/56; H04L-029/06
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

**7/5/12 (Item 12 from file: 350)**



014113146 **Image available**
WPI Acc No: 2001-597358/200168
XRPX Acc No: N01-445386

**Data transfer system for network processor, forwards data between memory chips relevant to edges of clock such that data is recorded and reproduced from specific memory banks within set time**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); IBM CORP (IBMC )
Inventor: BASS B M; CALVIGNAC J L; **HEDDES M C** ; JENKINS S K; SIEGEL M S; TROMBLEY M R; VERPLANKEN F J
Number of Countries: 006 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| CA 2316122 | A1 | 20010704 | CA 2316122 | A | 20000817 | 200168 | B |
| CN 1303050 | A | 20010711 | CN 2000137002 | A | 20001227 | 200168 | |
| JP 2001222465 | A | 20010817 | JP 2000390789 | A | 20001222 | 200168 | |
| KR 2001070356 | A | 20010725 | KR 200082481 | A | 20001227 | 200208 | |
| SG 90222 | A1 | 20020723 | SG 20007697 | A | 20001228 | 200257 | |
| US 6473838 | B1 | 20021029 | US 2000477576 | A | 20000104 | 200274 | |

Priority Applications (No Type Date): US 2000477576 A 20000104
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| CA 2316122 | A1 | E | 14 | G11C-007/10 | |
| CN 1303050 | A | | | G06F-012/00 | |
| JP 2001222465 | A | | 9 | G06F-012/06 | |
| KR 2001070356 | A | | | G06F-013/00 | |
| SG 90222 | A1 | | | G06F-012/02 | |
| US 6473838 | B1 | | | G06F-012/00 | |

Abstract (Basic): CA 2316122 A1

NOVELTY - The data is transferred between double data rate dynamic random access memory (DDR DRAM) chips in parallel based on the rising and falling edges of the time clock. Each network processor reads and writes the four memory banks of data allowed during one 20 cycle cell of the time clock.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Method of storing and transferring data between processors;

(b) High bandwidth data arbitration method for network processor;

(c) Randomized read and write access instruction provision method

for network processor
USE - For network processors in computer network.
ADVANTAGE - Enables providing wide bandwidth data transfer in randomized manner, thereby accessing of control information is improved.
DESCRIPTION OF DRAWING(S) - The figure shows the timing diagram of DRAM chip.
pp; 14 DwgNo 1/1
Title Terms: DATA; TRANSFER; SYSTEM; NETWORK; PROCESSOR; FORWARD; DATA; MEMORY; CHIP; RELEVANT; EDGE; CLOCK; DATA; RECORD; REPRODUCE; SPECIFIC; MEMORY; BANK; SET; TIME
Derwent Class: T01; U14
International Patent Class (Main): G06F-012/00; G06F-012/02; G06F-012/06; G06F-013/00; G11C-007/10
International Patent Class (Additional): G06F-013/38; **G06F-015/167** ; H04L-012/28
File Segment: EPI

**7/5/13 (Item 13 from file: 350)**


014112037 **Image available**
WPI Acc No: 2001-596249/200167
XRPX Acc No: N01-444490

**Data flow managing apparatus for internet, has indicators indicating data format and starting address, to processing units, when input information is processed**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); IBM UK LTD (IBMC )
Inventor: BASS B M; CALVIGNAC J L; DAVIS G T; GALLO A M; **HEDDES M** ; JENKINSS S K; LEAVENS R B; SIEGEL M S; VERPLANKEN F J; JENKINS S K
Number of Countries: 091 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200150259 | A1 | 20010712 | WO 2000GB4950 | A | 20001221 | 200167 | B |
| AU 200120166 | A | 20010716 | AU 200120166 | A | 20001221 | 200169 | |
| BR 200015717 | A | 20020723 | BR 200015717 | A | 20001221 | 200257 | |
| | | | WO 2000GB4950 | A | 20001221 | | |
| CZ 200201442 | A3 | 20020717 | WO 2000GB4950 | A | 20001221 | 200260 | |
| | | | CZ 20021442 | A | 20001221 | | |
| EP 1244964 | A1 | 20021002 | EP 2000983409 | A | 20001221 | 200265 | |
| | | | WO 2000GB4950 | A | 20001221 | | |
| KR 2002071911 | A | 20020913 | KR 2002708455 | A | 20020628 | 200311 | |

Priority Applications (No Type Date): US 2000479028 A 20000107; US 2000479027 A 20000107
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200150259 | A1 | E | 66 | G06F-009/46 | |

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

| | | | | |
|---|---|---|---|---|
| AU 200120166 | A | | G06F-009/46 | Based on patent WO 200150259 |
| BR 200015717 | A | | G06F-009/46 | Based on patent WO 200150259 |
| CZ 200201442 | A3 | | G06F-009/46 | Based on patent WO 200150259 |
| EP 1244964 | A1 | E | G06F-009/46 | Based on patent WO 200150259 |

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

| | | | | |
|---|---|---|---|---|
| KR 2002071911 | A | | H04L-012/56 | |

Abstract (Basic): WO 200150259 A1
NOVELTY - Processing units coupled to dispatcher and internal data memory are fabricated on a substrate. A classifier coupled to the dispatcher, has a comparison unit for determining data format for the

input information and to store it in internal memory. Indicators indicating the data format and starting address are generated during data processing. A completion unit receives the processed information.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Input information processing method;
(b) Input frame identifying method;
(c) Information frame analyzing apparatus

USE - For internet.

ADVANTAGE - Allows quicker and more efficient processing of data packet and also allows the processed packets to be reassembled in the same order in which the packets are received and also allows processing of multiple data flows without influencing each other.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of interface device having embedded processor.

pp; 66 DwgNo 1/12

Title Terms: DATA; FLOW; MANAGE; APPARATUS; INDICATE; INDICATE; DATA; FORMAT; START; ADDRESS; PROCESS; UNIT; INPUT; INFORMATION; PROCESS

Derwent Class: T01; W01

International Patent Class (Main): **G06F-009/46** ; H04L-012/56

International Patent Class (Additional): H04L-029/06

File Segment: EPI

**7/5/14 (Item 14 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



014096372 **Image available**

WPI Acc No: 2001-580586/200165

XRPX Acc No: N01-432360

**Communication network apparatus for computers, has coupler which interconnects the upside and downside data paths through which egress data is routed at specific speed**

Patent Assignee: IBM CORP (IBMC ); INT BUSINESS MACHINES CORP (IBMC )

Inventor: BARKER K J; BASS B M; CALVIGNAC J; **HEDDES M C** ; SIEGEL M S; TROMBLEY M R; VERPLANKEN F J

Number of Countries: 023 Number of Patents: 005

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200116682 | A1 | 20010308 | WO 2000US20798 | A | 20000824 | 200165 | B |
| EP 1222517 | A1 | 20020717 | EP 2000957270 | A | 20000824 | 200254 | |
| | | | WO 2000US20798 | A | 20000824 | | |
| KR 2002026266 | A | 20020406 | KR 2002702334 | A | 20020222 | 200267 | |
| CN 1371495 | A | 20020925 | CN 2000812060 | A | 20000824 | 200305 | |
| JP 2003508951 | W | 20030304 | WO 2000US20798 | A | 20000824 | 200319 | |
| | | | JP 2001520572 | A | 20000824 | | |

Priority Applications (No Type Date): US 99384689 A 19990827

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200116682 | A1 | E | 78 | G06F-003/00 | |
| Designated States (National): CN JP KR SG | | | | | |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE | | | | | |
| EP 1222517 | A1 | E | | G06F-003/00 | Based on patent WO 200116682 |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE | | | | | |
| KR 2002026266 | A | | | G06F-015/00 | |
| CN 1371495 | A | | | G06F-003/00 | |
| JP 2003508951 | W | | 90 | H04L-012/56 | Based on patent WO 200116682 |

Abstract (Basic): WO 200116682 A1

NOVELTY - A media interface is attached to communication network or network device and control information is routed or processed by the processor (12). A coupler interconnects the upside and downside data paths through which egress data is routed from media interface to apparatus, and from apparatus to media interface at specific speed,

respectively.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Single chip apparatus;

(b) Control method of communication network apparatus

USE - For linking together information handling system or computers and for improving the data flow handling capacity of network switches.

ADVANTAGE - Enables to size support capabilities to a range of potential demands, while improving the speed of handling of data being transferred. Enables to increase the amount of data handling.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of interface device.

Processor (12)

pp; 78 DwgNo 1/18

Title Terms: COMMUNICATE; NETWORK; APPARATUS; COMPUTER; COUPLE; INTERCONNECT; UPSIDE; DATA; PATH; THROUGH; EGRESS; DATA; ROUTE; SPECIFIC; SPEED

Derwent Class: T01; W01

International Patent Class (Main): G06F-003/00; **G06F-015/00** ; H04L-012/56

International Patent Class (Additional): G06F-013/00; **G06F-015/16**

File Segment: EPI

**7/5/15 (Item 15 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



013956871 **Image available**

WPI Acc No: 2001-441085/200147

XRPX Acc No: N01-326321

**Scalable switch apparatus for use in data communication network, has processing units operating simultaneously to carry out task associated with assigned input information units**

Patent Assignee: IBM CORP (IBMC ); INT BUSINESS MACHINES CORP (IBMC )

Inventor: BASS B M; CALVIGNAC J; GALLO A M; **HEDDES M C** ; LEAVENS R B; PATEL P C; RINALDI M A; SIEGEL M S; VERPLANKEN F J

Number of Countries: 023 Number of Patents: 005

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200116777 | A1 | 20010308 | WO 2000US20797 | A | 20000824 | 200147 | B |
| EP 1226509 | A1 | 20020731 | EP 2000957269 | A | 20000824 | 200257 | |
| | | | WO 2000US20797 | A | 20000824 | | |
| KR 2002026265 | A | 20020406 | KR 2002702310 | A | 20020222 | 200267 | |
| CN 1371500 | A | 20020925 | CN 2000812061 | A | 20000824 | 200305 | |
| JP 2003508957 | W | 20030304 | WO 2000US20797 | A | 20000824 | 200319 | |
| | | | JP 2001520661 | A | 20000824 | | |

Priority Applications (No Type Date): US 99384691 A 19990827

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200116777 | A1 | E | 82 | G06F-015/00 | |
| Designated States (National): CN JP KR SG | | | | | |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE | | | | | |
| EP 1226509 | A1 | E | | G06F-015/00 | Based on patent WO 200116777 |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE | | | | | |
| KR 2002026265 | A | | | G06F-015/00 | |
| CN 1371500 | A | | | G06F-015/00 | |
| JP 2003508957 | W | | 94 | H04L-012/56 | Based on patent WO 200116777 |

Abstract (Basic): WO 200116777 A1

NOVELTY - Internal instruction and data memories respectively store instruction and information accessible to processing units in a substrate (10). A dispatcher pre fetches input information units which are assigned to processing units. which operate simultaneously to perform task associated with assigned input information units. A completion unit receives output information units from processing

units.

DETAILED DESCRIPTION - The completion unit orders the output information unit to maintain a predetermined sequence. A memory controller operatively interposed between the processing units and the internal data memory, provides simultaneous access to data memory, in response to simultaneous requests from processing units. INDEPENDENT CLAIMS are included for the following:

(a) Scalable switch apparatus operating method;

(b) Information handling system

USE - For use in data communication network.

ADVANTAGE - Provides scalable switch architecture which is capable of sizing support capabilities to a range of potential demands while improving the speed of handling of data being transferred. Improves the data flow handling capability of network switches.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of interface device.

Substrate (10)

pp; 82 DwgNo 1/18

Title Terms: SWITCH; APPARATUS; DATA; COMMUNICATE; NETWORK; PROCESS; UNIT; OPERATE; SIMULTANEOUS; CARRY; TASK; ASSOCIATE; ASSIGN; INPUT; INFORMATION ; UNIT

Derwent Class: T01

International Patent Class (Main): **G06F-015/00** ; H04L-012/56

International Patent Class (Additional): **G06F-015/16**

File Segment: EPI

**7/5/16 (Item 16 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



013956864 **Image available**

WPI Acc No: 2001-441078/200147

Related WPI Acc No: 2001-389579; 2001-441055; 2001-441056; 2001-441058; 2001-441059; 2001-441060; 2001-441061; 2001-441064

XRPX Acc No: N01-326314

**Multifunctional interface has control point processor that directs exchange of data between input, output ports and data flows through memory**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )

Inventor: BASS B M; CALVIGNAC J L; GALLO A M; **HEDDES M C** ; RAO S; SIEGEL M S; VERPLANKEN F J; YOUNGMAN B A

Number of Countries: 023 Number of Patents: 004

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200116763 | A1 | 20010308 | WO 2000US20795 | A | 20000824 | 200147 | B |
| EP 1226501 | A1 | 20020731 | EP 2000959158 | A | 20000824 | 200257 | |
| | | | WO 2000US20795 | A | 20000824 | | |
| KR 2002024330 | A | 20020329 | KR 2002702312 | A | 20020222 | 200265 | |
| JP 2003508954 | W | 20030304 | WO 2000US20795 | A | 20000824 | 200319 | |
| | | | JP 2001520649 | A | 20000824 | | |

Priority Applications (No Type Date): US 99384692 A 19990827

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200116763 | A1 | E | 81 | G06F-013/00 | |
| Designated States (National): CN JP KR SG | | | | | |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE | | | | | |
| EP 1226501 | A1 | E | | G06F-013/00 | Based on patent WO 200116763 |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE | | | | | |
| KR 2002024330 | A | | | G06F-013/00 | |
| JP 2003508954 | W | | 94 | H04L-012/56 | Based on patent WO 200116763 |

Abstract (Basic): WO 200116763 A1

NOVELTY - A control point processor loads in structure to be executed by interface processors, to direct exchange of data between the ports and data flow through data memory.

DETAILED DESCRIPTION - The communication device consists of control point processor subsystem and a network processor. The device also includes interface processor, media interfaces, queue registers. Control point processor generates a guided frame with information and forwards to media interfaces. INDEPENDENT CLAIMS are also included for the following:

(a) Communication device;

(b) Data flow directing method

USE - Used for link information handling systems. Used for data flow handling capability of network switches.

ADVANTAGE - Storage facility for the embedded processing complex. Provides scalable switch architecture for sizing support capabilities to a range of potential demands and improving speed of data transfer.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of interface.

pp; 81 DwgNo 1/18

Title Terms: MULTIFUNCTION; INTERFACE; CONTROL; POINT; PROCESSOR; DIRECT; EXCHANGE; DATA; INPUT; OUTPUT; PORT; DATA; FLOW; THROUGH; MEMORY

Derwent Class: T01

International Patent Class (Main): G06F-013/00; H04L-012/56

International Patent Class (Additional): G06F-013/38; **G06F-015/00** ; **G06F-015/16** ; **G06F-015/173** ; **G06F-015/177** ; **G06F-015/76**

File Segment: EPI

**7/5/17 (Item 17 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



013882917 **Image available**

WPI Acc No: 2001-367130/200138

XRPX Acc No: N01-267909

**Scalable network switching apparatus has control point processor that loads into memory instructions to be executed by interface processors in directing exchange of data between input and output ports**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); ALLEN J J (ALLE-I); BASS B M (BASS-I); CALVIGNAC J L (CALV-I); GAUR S P (GAUR-I); HEDDES M C (HEDD-I); SIEGEL M S (SIEG-I); VERPLANKEN F J (VERP-I)

Inventor: ALLEN J; BASS B M; CALVIGNAC J L; GAUR S P; **HEDDES M C** ; SIEGEL M S; VERPLANKEN F J; ALLEN J J

Number of Countries: 024 Number of Patents: 008

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200117179 | A1 | 20010308 | WO 2000US20796 | A | 20000824 | 200138 | B |
| US 20020048270 | A1 | 20020425 | US 99384747 | A | 19990827 | 200233 | |
| | | | US 20013981 | A | 20011023 | | |
| US 20020061022 | A1 | 20020523 | US 99384747 | A | 19990827 | 200239 | |
| | | | US 20012932 | A | 20011023 | | |
| EP 1208676 | A1 | 20020529 | EP 2000959159 | A | 20000824 | 200243 | |
| | | | WO 2000US20796 | A | 20000824 | | |
| US 6404752 | B1 | 20020611 | US 99384747 | A | 19990827 | 200244 | |
| KR 2002027570 | A | 20020413 | KR 2002702309 | A | 20020222 | 200267 | |
| CN 1369160 | A | 20020911 | CN 2000811558 | A | 20000824 | 200282 | |
| JP 2003508967 | W | 20030304 | WO 2000US20796 | A | 20000824 | 200319 | |
| | | | JP 2001521005 | A | 20000824 | | |

Priority Applications (No Type Date): US 99384747 A 19990827; US 20013981 A 20011023; US 20012932 A 20011023

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200117179 | A1 | E | 81 | H04L-012/56 | |
| Designated States (National): CN JP KR SG | | | | | |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE | | | | | |
| US 20020048270 | A1 | | | H04L-012/56 | Div ex application US 99384747 |
| US 20020061022 | A1 | | | H04L-012/56 | Cont of application US 99384747 |
| EP 1208676 | A1 | E | | H04L-012/56 | Based on patent WO 200117179 |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI | | | | | |

LU MC NL PT SE
US 6404752 B1 H04L-012/28
KR 2002027570 A H04L-012/00
CN 1369160 A H04L-012/56
JP 2003508967 W 93 H04L-012/56 Based on patent WO 200117179

Abstract (Basic): WO 200117179 A1
NOVELTY - A control point processor cooperates with an interface device by loading into instruction memory instructions to be executed by interface processors (12) in directing the exchange of data between input and output ports and the flow of data through the data memory. The interface devices are operatively connected with each of the input and output ports of a switching fabric device.
DETAILED DESCRIPTION - The interface devices are connected to a switching fabric device and the control point processor. Each interface device includes interface processors formed on a substrate (10). Internal instruction memory and data memory are also formed on the substrate. The input and output ports are formed on the substrate.
INDEPENDENT CLAIMS are also included for the following:
(a) a scalable network processor;
(b) and a network switching method.
USE - Used for linking together information handling systems or computers of various types and capabilities. Used in data communication network.
ADVANTAGE - Enables sizing support capabilities to a range of potential demands while improving the speed of handling of data being transferred. Provides rate switching of frames that include layer 2, layer 3, layer 4 and layer 5. Allows protocols to be switched at greater speeds using hardware. Allows system administrators the ability to configure features such as grouping ports into separate domains or trunks.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the interface device.
Substrate (10)
Interface processors (12)
pp; 81 DwgNo 1/18
Title Terms: NETWORK; SWITCH; APPARATUS; CONTROL; POINT; PROCESSOR; LOAD; MEMORY; INSTRUCTION; EXECUTE; INTERFACE; PROCESSOR; DIRECT; EXCHANGE; DATA; INPUT; OUTPUT; PORT
Derwent Class: T01; W01; W02
International Patent Class (Main): H04L-012/00; H04L-012/28; H04L-012/56
International Patent Class (Additional): **G06F-015/16** ; **G06F-015/177** ; H04J-003/24; H04Q-011/04
File Segment: EPI

**7/5/18 (Item 18 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


009909839 **Image available**
WPI Acc No: 1994-177545/199422
XRPX Acc No: N94-139839
**Content addressable memory implementation using RAM - divides RAM into locations addressable by sub-words of keyword, connects address lines of memory locations to subset of keyword input lines, and passes output of memory locations to AND-gate to activate subset of matching lines**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: **HEDDES M C A**
Number of Countries: 006 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 600139 | A1 | 19940608 | EP 92810952 | A | 19921204 | 199422 | B |
| US 5450351 | A | 19950912 | US 93154765 | A | 19931119 | 199542 | N |

Priority Applications (No Type Date): EP 92810952 A 19921204; US 93154765 A 19931119
Cited Patents: EP 228917

Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
EP 600139     A1 E  11 G06F-015/409
   Designated States (Regional): CH DE FR GB LI
US 5450351    A     10 G11C-015/00

Abstract (Basic): EP 600139 A
A content addressable memory (CAM) implementation for a W-bit wide keyboard, applied to a set of input lines, has a set of N possible matching lines with a random access memory - RAM - addressable by the keyword.
The RAM consists of m individually-addressable memory units each having an N-bit wide output. The address lines of the memory units are connected to a subset of the input lines for the keyword.
The outputs of the memory units are connected to a gate performing a bit-wise AND operation. The output serves to activate a subset of the N possible matching lines.
USE/ADVANTAGE - In computer keyboards. High search speed. Wide address space.
Dwg.2/5
Title Terms: CONTENT; ADDRESS; MEMORY; IMPLEMENT; RAM; DIVIDE; RAM; LOCATE; ADDRESS; SUB; WORD; KEYWORD; CONNECT; ADDRESS; LINE; MEMORY; LOCATE; SUBSET; KEYWORD; INPUT; LINE; PASS; OUTPUT; MEMORY; LOCATE; AND-GATE; ACTIVATE; SUBSET; MATCH; LINE
Derwent Class: T01
International Patent Class (Main): **G06F-015/409** ; G11C-015/00
File Segment: EPI

**7/5/19 (Item 19 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS


01552693
**METHOD AND SYSTEM FOR PERFORMING A PATTERN MATCH SEARCH FOR TEXT STRINGS**
**VERFAHREN UND SYSTEM ZUM AUSFUHREN EINER SUCHE VON MUSTERERKENNUNG FUR TEXTZEICHENREIHEN**
**PROCEDE ET SYSTEME PERMETTANT D'EFFECTUER UNE RECHERCHE D'APPARIEMENT DE FORMES DE CHAINES DE TEXTES**
PATENT ASSIGNEE:
International Business Machines Corporation, (200128), New Orchard Road, Armonk, NY 10504, (US), (Applicant designated States: all)
INVENTOR:
BASSO, Claude, 7604 Percy Court, Raleigh, NC 27613, (US)
CALVIGNAC, Jean, Louis, 112 Spring Hollow Lane, Cary, NC 27511, (US)
**DAMON, Philippe** , 1000 Smith Level Road, Apt. V8, Carrboro, NC 27510, (US)
DAVIS, Gordon, Taylor, 97603 Franklin Ridge, Chapel Hill, NC 27514, (US)
**HEDDES, Marco** , 108 Saint Lenville Drive, Cary, NC 27511, (US)
JEFFRIES, Clark, Debs, 2806 H Bainbridge Drive, Durham, NC 27713, (US
PATENT (CC, No, Kind, Date):
WO 2003005288 030116
APPLICATION (CC, No, Date): EP 2002730512 020618; WO 2002GB2762 020618
PRIORITY (CC, No, Date): US 898253 010703
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06K-009/00
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 030312 A2 International application. (Art. 158(1))
Application: 030312 A2 International application entering European phase
LANGUAGE (Publication,Procedural,Application): English; English; English

**7/5/20 (Item 20 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

01490864
**HIGH SPEED NETWORK PROCESSOR**
**PROCESSEUR DE RESEAU HAUTE VITESSE**
PATENT ASSIGNEE:
International Business Machines Corporation, (200128), New Orchard Road, Armonk, NY 10504, US\(Applicant designated states: , AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LU; NL; PT; SE; TR; LI)
Compagnie IBM France, (238333), Tour Descartes, 2, avenue Gambetta, 92066 Paris La Defense Cedex, FR\(Applicant designated states: , MC)
INVENTOR:
CALVIGNAC, Jean, Louis, 112 Spring Hollow Lane, Cary, NC 27511, (US)
GOETZINGER, William, John, 605 Cortland Lane SW, Rochester, MN 55902-2219 , (US)
HANDLOGTEN, Glen, Howard, 4426 Cambridge Lane NW, Rochester, NY 55901, (US)
**HEDDES, Marco, C.** , 108 Saint Lenville Drive, Cary, NC 27511, (US)
LOGAN, Joseph, Franklin, 4005 Westwood Place, Raleigh, NC 27613, (US)
MIKOS, James, Francis, 4612 Birdie Lane NW, Rochester, MN 55901, (US)
NORGAARD, David, Alan, 1425 Wilshire Woods Lane NE, Rochester, MN 55906, (US)
VERPLANKEN, Fabrice, 9152 Route de Cagnes, F-06610 La Gaude, (FR
PATENT (CC, No, Kind, Date):
WO 2002071206 020912
APPLICATION (CC, No, Date): EP 2002719909 020131; WO 2002EP1955 020131
PRIORITY (CC, No, Date): US 273438 P 010305
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-009/00**
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 021106 A2 International application. (Art. 158(1))
Application: 021106 A2 International application entering European phase
LANGUAGE (Publication,Procedural,Application): English; English; English

**7/5/21 (Item 21 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS


01463693
**AN EFFICIENT TIMER MANAGEMENT SYSTEM**
**EFFIZIENTES VERWALTUNGSYSTEM EINES ZEITGEBERS**
**UN SYSTEME EFFICACE DE GESTION DE MINUTERIE**
PATENT ASSIGNEE:
International Business Machines Corporation, (200128), New Orchard Road, Armonk, NY 10504, (US), (Applicant designated States: all)
INVENTOR:
**DAMON, Philipe** , 1000 Smith Level Road Apt S8, Carrboro, NC 27510, (US)
**HEDDES, Marco** , 4109 Grand Manor Court 308, Raleigh, NC 27612, (US
PATENT (CC, No, Kind, Date):
WO 2002027468 020404
APPLICATION (CC, No, Date): EP 2001970009 010927; WO 2001GB4322 010927
PRIORITY (CC, No, Date): US 675545 000928
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-009/00**
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 021016 A2 International application. (Art. 158(1))
Application: 021016 A2 International application entering European phase
LANGUAGE (Publication,Procedural,Application): English; English; English

**7/5/22 (Item 22 from file: 347)**
DIALOG(R)File 347:JAPIO

07189288 **Image available**
MEMORY MANAGEMENT METHOD AND SYSTEM IN NETWORK PROCESSING SYSTEM

PUB. NO.: 2002-057688 [JP 2002057688 A]
PUBLISHED: February 22, 2002 (20020222)
INVENTOR(s): GALLO ANTHONY MATTEO
HARIHARAN SEETA
**HEDDES MARCO C**
SURIDARU RAAO
VERRILLI COLIN BEATON
GAIL EILEEN WOODLAND
APPLICANT(s): INTERNATL BUSINESS MACH CORP (IBM)
APPL. NO.: 2001-104637 [JP 20011104637]
FILED: April 03, 2001 (20010403)
PRIORITY: 00 546653 [US 2000546653], US (United States of America), April 10, 2000 (20000410)
INTL CLASS: H04L-012/46; G06F-012/02; G06F-012/06; **G06F-015/167** ; H04L-012/44; H04L-012/56

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method and a system for managing a memory in a network processing system for providing the allocation of a physical memory section inside a network processor connected to a control point processor by a bus.

SOLUTION: This allocation system provides a memory management layer without the need of a complete operating system interface and supports the asynchronous completion of allocation requests. Multicast allocation is supported and the allocation can be simultaneously requested on the plural network processors. An allocation mechanism returns a token, then a memory position is accessed by a protocol through the bus by using the token, and the allocation performed on the plural network processors where actual physical addresses and memory constitution are different is referred to by a single token.



**7/5/23 (Item 23 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00975326 **Image available**
**METHOD AND SYSTEM FOR PERFORMING A PATTERN MATCH SEARCH FOR TEXT STRINGS**
**PROCEDE ET SYSTEME PERMETTANT D'EFFECTUER UNE RECHERCHE D'APPARIEMENT DE FORMES DE CHAINES DE TEXTES**

Patent Applicant/Assignee:
INTERNATIONAL BUSINESS MACHINES CORPORATION, New Orchard Road, Armonk, NY 10504, US, US (Residence), US (Nationality)
IBM UNITED KINGDOM LIMITED, P.O. Box 41, North Harbour, Portsmouth, Hampshire PO6 3AU, GB, GB (Residence), GB (Nationality), (Designated only for: MG)
Inventor(s):
BASSO Claude, 7604 Percy Court, Raleigh, NC 27613, US,
CALVIGNAC Jean Louis, 112 Spring Hollow Lane, Cary, NC 27511, US,
**DAMON Philippe** , 1000 Smith Level Road, Apt. V8, Carrboro, NC 27510, US,
DAVIS Gordon Taylor, 97603 Franklin Ridge, Chapel Hill, NC 27514, US,
**HEDDES Marco** , 108 Saint Lenville Drive, Cary, NC 27511, US,
JEFFRIES Clark Debs, 2806 H Bainbridge Drive, Durham, NC 27713, US
Legal Representative:
LITHERLAND David Peter (agent), IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester, Hampshire SO21 2JN, GB,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200305288 A2 20030116 (WO 0305288)
Application: WO 2002GB2762 20020618 (PCT/WO GB0202762)

Priority Application: US 2001898253 20010703
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU
CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO
RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G06K-009/00
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 6298

English Abstract
A method and system is disclosed for performing a pattern match search for a data string having a plurality of characters separated by delimiters. A search key is constructed by generating a full match search increment comprising the binary representation of a data string element, wherein the data string element comprises all characters between a pair of delimiters. The search key is completed by concatenating a pattern search prefix to the full match search increment, wherein the pattern search prefix is a cumulative pattern search result of each previous full match search increment. A full match search is then performed within a lookup table utilizing the search key. In response to finding a matching pattern within the lookup table, the process returns to constructing a next search key. In response to not finding a matching pattern, the previous full match search result is utilized to process the data string.

French Abstract
L'invention concerne un procede et un systeme permettant d'effectuer une recherche d'appariement de formes d'une chaine de donnees possedant une pluralite de caracteres separes par des delimiteurs. Une cle de recherche est construite par generation d'un increment de recherche a appariement total comprenant la representation binaire d'un element de la chaine de donnees, cet element comprenant tous les caracteres compris entre une paire de delimiteurs. La cle de recherche est completee par enchainement d'un prefixe de recherche de formes a l'increment de recherche d'appariement total, ce prefixe etant un resultat de recherche de formes cumulatif de chaque increment de recherche d'appariement total anterieur. Une recherche d'appariement total est ensuite effectuee dans une table de recherche par mise en oeuvre de la cle de recherche. En reponse au fait d'avoir trouve une forme d'appariement dans la table de recherche, le procede comprend une etape consistant a construire une cle de recherche suivante. En reponse au fait de ne pas avoir trouve de forme d'appariement, le resultat de recherche d'appariement total anterieur est mis en oeuvre pour traiter la chaine de donnees.

Legal Status (Type, Date, Text)
Publication 20030116 A2 Without international search report and to be republished upon receipt of that report.
Examination 20030213 Request for preliminary examination prior to end of 19th month from priority date

```
Set     Items   Description
S1     261219   API OR APPLICATION()PROGRAM?()INTERFACE? OR (APPLICATION? -
            OR PROGRAM?)(2W)INTERFACE?
S2      38941   (TIME()DEPENDENT? OR SYNCHRON?) AND (ASYNCHRON? OR (NON OR
            "NOT")()SYNCHRONOUS)
S3    1279791   TIMER? OR TIMING OR TIMESTAMP? OR INTERVAL? OR CLOCK?
S4    7611050   END? ? OR TIMEOUT? OR TIME()OUT? ? OR EXPIR?
S5       6297   S3(3N)(DATABASE? OR DATA()(BASE? OR BANK? OR FILE?) OR DAT-
            ABANK? OR DATAFILE? OR TABLE?)
S6     593522   STATEMACHINE? OR STATE()MACHINE? OR CONTROLLER?
S7       1154   INITILIALI? OR REINITIALI?
S8      55521   S3(3N)(MANAG? OR CONTROL? OR ADMINIST? OR MONITOR? OR TRAC-
            K?)
S9          0   S1(S)S2(S)S5
S10         5   S1(S)S5
S11        43   S1(S)S2(S)S3
S12       204   S1(S)S8
S13         6   S12(S)(S6 OR S7)(S)S4
S14        53   S10 OR S11 OR S13
S15        38   RD (unique items)
S16        30   S15 NOT PY>2000
S17        29   S16 NOT PD>20000928
File 275:Gale Group Computer DB(TM) 1983-2003/Apr 04
         (c) 2003 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2003/Apr 03
         (c) 2003 The Gale group
File 636:Gale Group Newsletter DB(TM) 1987-2003/Apr 04
         (c) 2003 The Gale Group
File  16:Gale Group PROMT(R) 1990-2003/Apr 04
         (c) 2003 The Gale Group
File 624:McGraw-Hill Publications 1985-2003/Apr 07
         (c) 2003 McGraw-Hill Co. Inc
File 484:Periodical Abs Plustext 1986-2003/Mar W5
         (c) 2003 ProQuest
File 613:PR Newswire 1999-2003/Apr 07
         (c) 2003 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 141:Readers Guide 1983-2003/Feb
         (c) 2003 The HW Wilson Co
File 696:DIALOG Telecom. Newsletters 1995-2003/Apr 07
         (c) 2003 The Dialog Corp.
File 621:Gale Group New Prod.Annou.(R) 1985-2003/Apr 04
         (c) 2003 The Gale Group
File 674:Computer News Fulltext 1989-2003/Apr W1
         (c) 2003 IDG Communications
File 369:New Scientist 1994-2003/Mar W4
         (c) 2003 Reed Business Information Ltd.
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File  15:ABI/Inform(R) 1971-2003/Apr 05
         (c) 2003 ProQuest Info&Learning
File   9:Business & Industry(R) Jul/1994-2003/Apr 04
         (c) 2003 Resp. DB Svcs.
File  13:BAMP 2003/Mar W4
         (c) 2003 Resp. DB Svcs.
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 610:Business Wire 1999-2003/Apr 07
         (c) 2003 Business Wire.
File 647:CMP  Computer Fulltext 1988-2003/Mar W3
         (c) 2003 CMP Media, LLC
File  98:General Sci Abs/Full-Text 1984-2003/Feb
         (c) 2003 The HW Wilson Co.
File 148:Gale Group Trade & Industry DB 1976-2003/Apr 04
         (c)2003 The Gale Group
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**17/3,K/1 (Item 1 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)


02118649 SUPPLIER NUMBER: 19958185 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**ExactTime for PC clocks.(PC Tech: Utilities) (Product Information)(Column)**
Petzold, Charles
PC Magazine, v16, n20, p291(4)
Nov 18, 1997
DOCUMENT TYPE: Column ISSN: 0888-8507 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 4433 LINE COUNT: 00345

ABSTRACT: ExactTime, a utility that automatically adjusts the PC's **clock** by calling one of two time-of-day services designed specifically for data use and...

...and time. It is a completely new, 32-bit program that relies on the atomic **clocks** of the National Institute of Standards and Technology and US Naval Observatory. Users install the...

...A detailed technical description of the program's operation is presented; it calls 14 Telephony **API** functions to manage the communications port and **synchronize** the PC **clock** with received data.

**17/3,K/2 (Item 2 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)


01942999 SUPPLIER NUMBER: 18345980 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Quickturn raises emulation stakes. (Quickturn Design Systems' Quest II verification software)(Product Announcement)**
Erkanat, Judy
Electronic News (1991), v42, n2118, p34(1)
May 27, 1996
DOCUMENT TYPE: Product Announcement ISSN: 1061-6624 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 879 LINE COUNT: 00074

... 0); an improved debugger; and a wide range of design-analysis tools.
It creates a **timing** -correct emulation model for a variety of design-style types ( **synchronous** and **asynchronous** ) and maps single-and multi-ported memories into the emulator. A new **programmable** target-**interface** module substantially eases the time and effort required to interface the emulated design to the...

**17/3,K/3 (Item 3 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)


01675335 SUPPLIER NUMBER: 15084067 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Cypress samples ATM part, broadens FIFO line. (Cypress Semiconductor Corp.'s CY7B951 SONET/SDH Serial Transceiver and CY7C455, CY7C456 and CY7C457 first-in, first-out memory chips; asynchronous transfer mode) (Product Announcement)**
DeTar, Jim
Electronic News (1991), v40, n2006, p46(1)
March 21, 1994
DOCUMENT TYPE: Product Announcement ISSN: 1061-6624 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 763 LINE COUNT: 00061

...ABSTRACT: Cypress CY7B951 SONET/SDH Serial transceiver (SST), which provides a reliable physical layer interface for **asynchronous** transfer mode (ATM), **synchronous** optical network (SONET) and **synchronous** digital

hierarchy (SDH) **applications** . The **interface** is made possible because of **clock** and data recovery from both 155.52 MHz and 51.84 MHz serial data streams...

...its general release in Apr 1994. The company also announces its CY7C455, CY7C456 and CY7C457 **clocked** first-in, first-out (FIFO) memory devices. In their PQFP packaging, these devices measure 10mm...

**17/3,K/4 (Item 4 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)


01674922 SUPPLIER NUMBER: 15056167 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**A Windows NT C++ class for asynchronous I/O. (programming techniques) (includes related articles on asynchronous input/output details and use of Win32 application programming interface synchronization objects) (Tutorial) (Technical)**
Tomlinson, Paula
Windows-DOS Developer's Journal, v5, n3, p25(14)
March, 1994
DOCUMENT TYPE: Technical ISSN: 1059-2407 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 5347 LINE COUNT: 00426

... fully preemptive, multithreaded operating system, one of the prices you pay is the complication of **synchronization** . Typical uses for **synchronization** include protecting shared data and serializing operations that depend upon the completion of other operations. The Win32 **API** on Windows NT supports several dedicated **synchronization** objects (mutexes, semaphores, events, and critical sections), but other handles can also be used as **synchronization** objects (processes, threads, files, console, **timers** , and more). A **synchronization** object is always in one of two states: signaled or not signaled. In general, threads...

**17/3,K/5 (Item 5 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)


01599235 SUPPLIER NUMBER: 13738308 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Sync comm controller. (Arnet Corp.'s SynCom/3000 communications co-processor board) (Brief Article) (Product Announcement)**
LAN Computing, v4, n5, p42(1)
May, 1993
DOCUMENT TYPE: Product Announcement ISSN: 1055-1808 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 95 LINE COUNT: 00008

... It features two individually programmable RS-422/485 ports, four channels of DMA, two programmable **timer clocks** and 1.2MB of onboard memory. It can be **programmed** to **interface** to almost any standard or proprietary **synchronous / asynchronous** protocol, including HDLC and IBM's BiSync, SDLC and SDLC Loop.
For more information, contact...

**17/3,K/6 (Item 6 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)


01493967 SUPPLIER NUMBER: 11713456 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Undocumented functions in Windows, part 1. (Microsoft Corp.'s Windows graphical user interface) (Lab Notes)(column) (Tutorial)**
Schulman, Andrew
PC Magazine, v11, n2, p315(10)
Jan 28, 1992
DOCUMENT TYPE: Tutorial ISSN: 0888-8507 LANGUAGE: ENGLISH

RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 8599 LINE COUNT: 00678

... message is what makes Windows multitasking non-preemptive.
Rather than hook INT 8 to get **timer** events, for instance, a Windows application uses the documented CreateTimer() **API** call to ask politely for **timer** messages. Even such **timer** messages present themselves **synchronously** , arriving only when the application asks for one by calling the GetMessage() function. Well regulated...

...it may be, however, this is not the behavior that many applications need from a **timer** or from other message sources, for that matter. Often an application needs to know about...
...in the middle of doing something else. Again, the solution is to use undocumented Windows **API** functions.
BEYOND THE API
Undocumented Windows API functions, messages, and data structures provide only part...

**17/3,K/7 (Item 7 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01442762 SUPPLIER NUMBER: 11071499 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Object-oriented Windows timers. (tutorial)**
Burk, Ron
TECH Specialist, v2, n7, p7(15)
July, 1991
DOCUMENT TYPE: tutorial ISSN: 1049-913X LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 3593 LINE COUNT: 00265

CAPTIONS: The Windows 3.0 **timer** **API** . ( **table** ); A C interface to timer objects. (program); A TPW timer object. (program)

**17/3,K/8 (Item 8 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01289560 SUPPLIER NUMBER: 07126822 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Drawing out DESQview power. (Quarterback Office Systems' DESQview application program interface)**
Hitt, Frederick J.
PC Tech Journal, v7, n4, p46(12)
April, 1989
ISSN: 0738-0194 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 8352 LINE COUNT: 00676

... values. Timer granularity is a true 1/100 of a second, obtained by reprogramming the **clock** chip hardware. **Table** 10 lists DESQview **API** calls associated with timer objects.
Programs can declare multiple timers, which can run concurrently, and ...

**17/3,K/9 (Item 9 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

01211547 SUPPLIER NUMBER: 05209294 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Real LU 6.2 over asynchronous communications? Yes, at last. (transparent links between layered architectures; connectivity section) (column)**
Mohen, Joe
PC Week, v4, n39, pC6(1)
Sept 29, 1987
DOCUMENT TYPE: column ISSN: 0740-1604 LANGUAGE: ENGLISH

RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 683 LINE COUNT: 00053

...ABSTRACT: come to fruition, although most strategic products from SNA vendors still combine the choice of **applications program interface** and user interface to the choice of link-level protocol. Emulators and communications software packages should include a configuration parameter to designate whether the link will be **synchronous** or **asynchronous** . Network Software Associates has developed a way to transmit SNA over **asynchronous** without protocol conversion. The new driver supports transmission in which the DTE does the **clocking** rather than the Data Communications Equipment; how the system works is described.

**17/3,K/10 (Item 10 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01210771 SUPPLIER NUMBER: 06085344 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Communications Manager APIs aid program developers; supports variety of links. (IBM hones a multifaceted network strategy.) (Section 2 Connectivity)**
Hindin, Eric
PC Week, v4, n46, pC1(2)
Nov 17, 1987
ISSN: 0740-1604 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1093 LINE COUNT: 00096

...ABSTRACT: non-IBM computers, through various types of links, including terminal emulation, and a number of **Applications Program Interfaces** (APIs), which will provide services applications can use to exchange data. The APIs also eliminate...

...write applications that function with specific communications hardware, allowing them to write directly to the **API** . This will make writing applications for OS-2 Extended Edition easier than writing to DOS...

...ability to run several applications concurrently, subject to the available hardware, available RAM, and the ' **timing** -sensitivity' of the applications.
... of communications applications centers around the "timing-sensitive" nature of the applications.
Because of their **timing** -sensitive nature, applications written to the Communications Manager's **asynchronous API** can execute alternately as users hot-key between applications, but not concurrently, because data traveling...

...ports can conflict. The ability to hot-key between applications is of limited use, since **asynchronous** applications usually involve communicating with a host over a public network. Such networks disconnect a user within a short period of time when no data is received. **Timing** problems also mandate that **synchronous** communications according to IBM's **Synchronous** Data Link Control (SDLC) protocol cannot occur concurrently with **asynchronous** applications.
Other limits on concurrent communications applications include a maximum of two links to IBM...

**17/3,K/11 (Item 1 from file: 47)**
DIALOG(R)File 47:Gale Group Magazine DB(TM)
(c) 2003 The Gale group. All rts. reserv.

05829964 SUPPLIER NUMBER: 63059110 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**INDUSTRY RESOURCES.**
Entertainment Design, 34, 6, 3
June, 2000
ISSN: 1520-5150 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 36203 LINE COUNT: 11269

... Clients include Aerosmith, Bush, Crystal Method, Morrissey, Paul Weller, Chicago, The Orb and Fiona Apple.

**API** (AUDIO PRODUCTS, INC.)
9017-C Mendenhall Ct., Columbia, MD 21045;
(b)410-381-7879; Fax...layout of theatrical stages, nightclubs, dance floors, restaurants and rock tours. Utilizing the built-in **database** , LD Assistant calculates candle power, beam angles and spreads with preset worksheets directly linked to...Francisco,
Munich, Tokyo, Hong Kong, Madrid and London.
Founded in 1982 in Budapest, Hungary.

GRAY **INTERFACES**
480C 36th Ave. SE, Calgary, AB T2G 1W4
Canada; (b)403-243-8110; Fax 416...

**17/3,K/12 (Item 2 from file: 47)**
DIALOG(R)File 47:Gale Group Magazine DB(TM)


05013536 SUPPLIER NUMBER: 19958165 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Open for business: Web storefront creation software. (12 electronic-commerce products reviewed) (includes related articles on elements of an electronic storefront, Editors' Choices, glossary, online-service and ISP templates, offering transaction security, business-to-business commerce) (Software Review)(Evaluation)**
Linthicum, David S.
PC Magazine, v16, n20, p143(19)
Nov 18, 1997
DOCUMENT TYPE: Evaluation ISSN: 0888-8507 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 12518 LINE COUNT: 00996

ABSTRACT: Twelve Internet-commerce tools are reviewed. Four of the **ten** are designed primarily for Web start-ups, while the others are suited to larger businesses...

...Store 3.0 is the Editors' Choice in the first category. It is the only **product** tested that is solely vendor-hosted and lets online newcomers build entire storefronts through a...
...is a good choice for Notes and Domino shops, but others will find it hard **to** use. Microsoft's Site Server 2.0 **provides** a sound **site** infrastructure, but requires more work to customize than other products.

**17/3,K/13 (Item 3 from file: 47)**
DIALOG(R)File 47:Gale Group Magazine DB(TM)


03019896 SUPPLIER NUMBER: 06085616 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Communications Manager APIs aid program developers; supports variety of links. (Applications Program Interfaces) (Connectivity: section 2)**
Hindin, Eric
PC Week, v4, n46, pC1(2)
Nov 17, 1987
LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1093 LINE COUNT: 00096

... of communications applications centers around the "timing-sensitive" nature of the applications.
Because of their **timing** -sensitive nature, applications written to the Communications Manager's **asynchronous API** can execute alternately as users hot-key between applications, but not concurrently, because data

traveling...

...ports can conflict. The ability to hot-key between applications is of limited use, since **asynchronous** applications usually involve communicating with a host over a public network. Such networks disconnect a user within a short period of time when no data is received. **Timing** problems also mandate that **synchronous** communications according to IBM's **Synchronous** Data Link Control (SDLC) protocol cannot occur concurrently with **asynchronous** applications.

Other limits on concurrent communications applications include a maximum of two links to IBM...

**17/3,K/14 (Item 1 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)


05321481 Supplier Number: 48100289 (USE FORMAT 7 FOR FULLTEXT)
**Lucent Single-Chip T1/E1 Said To Displace Six Chips**
Electronic News (1991), p020
Nov 3, 1997
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 344

... to minimize the occurrence of false lock conditions.
The T7630 is equipped with a user- **programmable** microprocessor **interface** that supports Intel and Motorola bus **timing** . Access to memory-mapped read and write registers is provided by an **asynchronous** parallel microprocessor port. Lucent's new T7630 comes in a 144-pin TQFP package and...

**17/3,K/15 (Item 2 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)


04564655 Supplier Number: 46709354 (USE FORMAT 7 FOR FULLTEXT)
**Nematron announces real-time computing capability for Microsoft Windows NT operating system**
News Release, pN/A
Sept 15, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1033

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...of a Virginia corporation which merged into Nematron in 1995. With the real-time Hyperkernel **API** , programmers can write applications that cooperate with standard Windows programs, like MS Office, while executing ...

...and measurement The Hyperkernel in conjunction with Windows NT enables devices such as robots, process **controllers** and motion control systems to be configured to execute as "nodes" or application servers on...

...standard Microsoft products including MS Visual C/C++. Specific features include the following: * High speed **timers** * Memory **management** * Interrupt handlers * Interprocess communication * File system services * Task scheduling and prioritization * Industrial network interfaces The... products that leverage or support its software. Nematron products cover a broad spectrum from low **end** operator interface to Windows NT control software, including PowerVIEW, AutoNet and FloPro. Nematron pioneered the ...

**17/3,K/16 (Item 3 from file: 16)**

DIALOG(R)File 16:Gale Group PROMT(R)
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04372967 Supplier Number: 46413269 (USE FORMAT 7 FOR FULLTEXT)
**Quickturn Raises Emulation Stakes**
Electronic News (1991), p034
May 27, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 817

... 0); an improved debugger; and a wide range of design-analysis tools.
It creates a **timing** -correct emulation model for a variety of design-style types ( **synchronous** and **asynchronous** ) and maps single- and multi-ported memories into the emulator. A new **programmable** target- **interface** module substantially eases the time and effort required to interface the emulated design to the...

**17/3,K/17 (Item 4 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
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04361015 Supplier Number: 46395840 (USE FORMAT 7 FOR FULLTEXT)
**Quickturn Announces Next-Generation Emulation Software and Verification Architecture; Next-generation architecture cuts time to emulation and enhances performance and debug/analysis capability.**
Business Wire, p5201104
May 20, 1996
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 1150

... performance improvement in the time required to compile incremental design changes. The software creates a **timing** -correct emulation model for a wide variety of design-style types ( **synchronous** and **asynchronous** ) and maps single- and multi-ported memories into the emulator. Moreover, a new **programmable** target- **interface** module substantially eases the time and effort required to interface the emulated design to the...

**17/3,K/18 (Item 5 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
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03339571 Supplier Number: 44621588 (USE FORMAT 7 FOR FULLTEXT)
**Real-time DOS does embedded act**
Electronic Engineering Times, p54
April 25, 1994
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 2004

... for desktop computing, it lacks real-time features, such as threads for multitasking, semaphores for **synchronization** , **timers** for **synchronous** deadline scheduling, interrupt-time memory management and a re-entrant **application program interface** ( **API** ). With some determination, we can overcome those problems and use DOS in real-time systems...

**17/3,K/19 (Item 6 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
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01481883 Supplier Number: 41794016 (USE FORMAT 7 FOR FULLTEXT)
**AT&T Unit Samples Modem Chip-Set**

Electronic News (1991), p17
Jan 14, 1991
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 318

... fully digital echo cancellation, the company said.
The data pump controller provides an internal universal **synchronous** / **asynchronous** receiver/transmitter (USART), a **programmable** **interface** (RS232C, host processor and US-ART), user registers, **clock** generation and control, and V.13 and V.54 support.
AT&T Micro also provides...

**17/3,K/20 (Item 1 from file: 160)**
DIALOG(R)File 160:Gale Group PROMT(R)


01835803
**ALTERA INTRODUCES FIRST USER-CONFIGURABLE MICROPROCESSOR PERIPHERAL DEVICE**
News Release October 5, 1987 p. 1

...operate with all popular 8-, 16- and 32-bit microprocessors at up to 25 MHz **clock** rates with zero wait states, and can easily and quickly be programmed to meet a...

... transceiver. In total 52 user-configurable storage elements are provided. Seven control macrocells can be **programmed** to **interface** the EPB1400 to all popular microprocessors with no external components. The 8-bit I/O...

... dual- feedback on all I/Os (allowing buried functions without wasting I/O pins); programmable **synchronous** and **asynchronous** **clocking** ; and multiple flip-flop types (D, JK, SR and T). Typical user-defined applications will include read/write counters and **timers** , parallel-serial and serial-parallel data converters, frequency dividers, data communications transceivers and configurable I...

**17/3,K/21 (Item 2 from file: 160)**
DIALOG(R)File 160:Gale Group PROMT(R)


01829882
**ALTERA INTRODUCES FIRST USER-CONFIGURABLE MICROPROCESSOR PERIPHERAL DEVICE DEVICE ELIMINATES NONRECURRING ENGINEERING COSTS AND SLASHES DEVELOPMENT TIME FOR CUS**
News Release November 4, 1987 p. 1

...operate with all popular 8-, 16- and 32-bit microprocessors at up to 25 MHz **clock** rates with zero wait states, and can easily and quickly be programmed to meet a...

... transceiver. In total 52 user-configurable storage elements are provided. Seven control macrocells can be **programmed** to **interface** the EPB1400 to all popular microprocessors with no external components. The 8-bit I/O...

... dual- feedback on all I/Os (allowing buried functions without wasting I/O pins); programmable **synchronous** and **asynchronous** **clocking** ; and multiple flip-flop types (D, JK, SR and T). Typical user-defined applications will include read/write counters and **timers** , parallel-serial and serial-parallel data converters, frequency dividers, data communications transceivers and configurable I...

**17/3,K/22 (Item 1 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)

00543938 91-18283
**Portable POSIX in Real Time**
Gallmeister, Bill
UNIX Review v9n4 PP: 32-36 Apr 1991
ISSN: 0742-3136 JRNL CODE: UXR

...ABSTRACT: CPU architectures, and it is available from a large number of vendors. While the UNIX **program interface** is quite general and elegant, it requires numerous and complicated extensions to support facilities crucial...

... 1. binary semaphores, 2. process memory locking, 3. shared memory, 4. priority scheduling facilities, 5. **asynchronous** event notification, 6. **timers** , 7. interprocess communications message passing, 8. **asynchronous** input-output (I-O), 9. **synchronized** I-O, and 10. real-time files.

**17/3,K/23 (Item 2 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)


00241350 84-19910
**SBC Includes On Board Operating System**
Wilson, Dave
Digital Design v14n5 PP: 47 May 1984
ISSN: 0147-9245 JRNL CODE: DDS

...ABSTRACT: designed to meet the needs of a broad range of applications that include multiprocessing, front- **end** processing, and stand-alone use. The CPU, an 80186, works in conjunction with the Intel...

... nucleus primitives for those applications that require a real-time executive, as well as providing **timers** and programmable interrupt **control** . There are 8 JEDEC 28-pin memory sites on the board. The parallel peripheral interface consists of three 8-bit parallel ports. The board also contains 2 **programmable** communication **interfaces** that use the Intel 8274 Multi-Protocol Serial **Controller** (MPSC). ...

**17/3,K/24 (Item 1 from file: 647)**
DIALOG(R)File 647:CMP Computer Fulltext


01016397 CMP ACCESSION NUMBER: EET19940425S1682
**Real-time DOS does embedded act**
STEVE JONES
ELECTRONIC ENGINEERING TIMES, 1994, n 794, 54
PUBLICATION DATE: 940425
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Embedded Systems
WORD COUNT: 2036

... for desktop computing, it lacks real-time features, such as threads for multitasking, semaphores for **synchronization** , **timers** for **synchronous** deadline scheduling, interrupt-time memory management and a re-entrant **application program interface** ( **API** ). With some determination, we can overcome those problems and use DOS in real-time systems...

**17/3,K/25 (Item 1 from file: 98)**
DIALOG(R)File 98:General Sci Abs/Full-Text

02770724 H.W. WILSON RECORD NUMBER: BGSI94020724
**Zeb: software for integration, display, and management of diverse environmental datasets.**
Corbet, Jonathan
Mueller, Cynthia; Burghart, Chris
Bulletin of the American Meteorological Society (Bull Am Meteorol Soc) v. 75 (May '94) p. 783-92
DOCUMENT TYPE: Product Evaluation
SPECIAL FEATURES: bibl il ISSN: 0003-0007
LANGUAGE: English
COUNTRY OF PUBLICATION: United States

...ABSTRACT: X-Y graphs, skew T plots, and time-height profiles. The fields for display, color **tables** , contour **intervals** , and various other display options are defined using an icon-based user interface. This highly ...

...for data handling. The library functions allow data storage, retrieval, and queries using a single **applications interface** , regardless of the data's source and organization. The software system runs under Unix and...

**17/3,K/26 (Item 1 from file: 148)**
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2003 The Gale Group. All rts. reserv.

10488445 SUPPLIER NUMBER: 21170496 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Lighting Controls for Energy Efficiency.**
Borden, Alfred R., IV
Energy User News, v23, n9, p25(1)
Sept, 1998
ISSN: 0162-9131 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1993 LINE COUNT: 00160

TEXT:
...The most common types are toggle switches, time clocks and photocells, relays, and contactors. Time **clocks** provide scheduled **control** of lighting loads. Photocells react to changes in the ambient light level. Both will continuously...

...device such as a microprocessor, photocell, or occupancy sensor. OCCUPANCY SENSORS An occupancy sensor lighting **controller** is a light switch that is designed to detect motion within a space. Upon detection... with incandescent lighting is a dimmer. A dimmer is typically considered an amenity for high- **end** spaces. However, dimmers offer an opportunity to conserve power usage. Modern dimmers are electronic and...
...rated life. Any space where incandescent lamps are used will benefit from dimmer installation. A **programmable** lighting **controller** , **interfaced** with the building automation computer, provides an excellent means for saving lighting energy. The control...

...Each lighting circuit is controlled by a relay that responds to the programmed directions. The **controller** can be fitted with several means for local override if people enter an area in...

**17/3,K/27 (Item 2 from file: 148)**
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2003 The Gale Group. All rts. reserv.

10222165 SUPPLIER NUMBER: 20641310 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**IC Advances Share The Spotlight With New Products At CeBIT 98.**
Vollmer, Alfred
Electronic Design, v46, n11, p72(1)
May 13, 1998
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 3004 LINE COUNT: 00238

TEXT:
...rate is not very high, it's sufficient for many applications. Philips estimates that the **end** -user starter price for a pair will be under $150, with a bill-of-materials...via a 400kHz (I.sup.2.C) bus, and the OTP which contains the customizable **application programming interface** ( **API** ), can be programmed in circuit via the (I.sup.2.C) bus. Speakerphone operation is...

...additional filters. This requires more RAM and ROM. A reference design as well as the **API** are also available. The reference board displayed at CeBIT used 64 kwords (128 kbytes) of...

...offers chip select for three chips. It integrates four general-purpose I/Os, a DMA **controller** , and FIFOs on a single chip. Power management modes D0, D1, and D3, as well...approval for its Network Termination (NT) evaluation board equipped with the new single-chip NT **controller** , NTC-Q (FEB 8091). The approval comes from the Chinese Research Institute for Thansmission Technology...

...special power management device (PMIC). The radio-frequency subsystem comprises four devices: a receiver front **end** (RF120), a transceiver (RF1S6), a power amplifier (RF130), and a power amplifier **controller** (RF122). The baseband processor unit integrates the ARM7 THUMB core, a DSP, a coprocessor, and...

...Packaged in a 10-pin TQFP, the integrated analog IC is a mixed-signal device **managing** all **timing** and signal conversion between the digital baseband subsystem and the analog voice I/O and...

...intends to introduce versions for GSM-1800 and the North American GSM-1900 by the **end** of this year, allowing for the realization of dual-band or multi- band GSM phones...

...application-specific frequencies. The RF13O amplifier for the GSM 900 needs a separate power amplifier **controller** , the RF122, which features an RF detector with a 60-dB dynamic range, error amplifier, integrator, and a gain shaper. The RF12O receiver front **end** integrates a low-noise amplifier with switchable gain and a mixer. All three devices are...

**17/3,K/28 (Item 3 from file: 148)**
DIALOG(R)File 148:Gale Group Trade & Industry DB


08370963 SUPPLIER NUMBER: 17943260 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Posix has leading role in open system.(Special Report: Embedded Systems) (Technology Information)**
Singh, Inder M.
Electronic Engineering Times, n881, p54(2)
Dec 18, 1995
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 989 LINE COUNT: 00083

...ABSTRACT: standard provides an excellent basis for creating embedded applications. The Posix standard outlines a Unix **API** and includes two extensions. Posix.1b outlines how to handle shared memory, priority scheduling, extended reliable signals, improved **timer** support and true **asynchronous** I/O. Posix.1c outlines the process for executing several threads in one Posix process...

**17/3,K/29 (Item 4 from file: 148)**
DIALOG(R)File 148:Gale Group Trade & Industry DB


08124425 SUPPLIER NUMBER: 17389671 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Plastics technology: manufacturing handbook & buyers' guide 1995/96.(Buyers Guide)**

Plastics Technology, v41, n8, pCOV(941)
August, 1995
DOCUMENT TYPE: Buyers Guide ISSN: 0032-1257 LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 174436 LINE COUNT: 15187

... and blending liquids, solids, or solid/liquid mixtures. Some models use rolling action and others **end** -over- **end** tumbling. Some have self-loading capability. Portable and stationary models use fixed- or variable-speed...Focus-2000 includes all features of Focus-100, but incorporates a Windows-based graphical user **interface** that simplifies system access by pointing to icons or list entries. System is compatible with...include nuclear, infrared, microwave, and caliper types. On-line control systems can link to temperature **controllers** , PLCs, and other systems. SPC available. IBM-compatible PC captures MIS data and links system..

```
Set     Items   Description
S1       3213   API OR APPLICATION()PROGRAM?()INTERFACE? OR (APPLICATION? -
            OR PROGRAM?)(2W)INTERFACE?
S2       5409   (TIME()DEPENDENT? OR SYNCHRON?) AND (ASYNCHRON? OR (NON OR
            "NOT")()SYNCHRONOUS)
S3     376286   TIMER? OR TIMING OR TIMESTAMP? OR INTERVAL? OR CLOCK?
S4    1675654   END? ? OR TIMEOUT? OR TIME()OUT? ? OR EXPIR?
S5       1224   S3(3N)(DATABASE? OR DATA()(BASE? OR BANK? OR FILE?) OR DAT-
            ABANK? OR DATAFILE? OR TABLE?)
S6     355160   STATEMACHINE? OR STATE()MACHINE? OR CONTROLLER?
S7      13036   INITIALI? OR REINITIAL?
S8      38465   MC=(T01-F01C? OR T01-J05B4P OR T01-S03?)
S9         14   S1 AND S2
S10         2   S1 AND S5
S11       148   S5 AND S6
S12         1   S11 AND S7
S13      1881   S2 AND S3
S14         7   S13 AND S5
S15         0   S8 AND S11
S16         8   S8 AND S13
S17        29   S9 OR S10 OR S12 OR S14 OR S16
S18        29   IDPAT (sorted in duplicate/non-duplicate order)
S19        29   IDPAT (primary/non-duplicate records only)
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200323
         (c) 2003 Thomson Derwent
```

19/5/1
DIALOG(R)File 350:Derwent WPIX


015138717 **Image available**
WPI Acc No: 2003-199243/200319
XRPX Acc No: N03-158461

**Redundant changeover apparatus for WDM based ring network, frames data output through changeover switch, based on** clock **signal input from PLL circuit receiving transmission frequency** clock **in output signal of switch**

Patent Assignee: FUJITSU LTD (FUIT ); IWAOKA T (IWAO-I); KOBAYASHI M (KOBA-I); KOYANO H (KOYA-I); TAKAIWA K (TAKA-I); TAKAYASU A (TAKA-I); TATENO M (TATE-I); YOSHINO Y (YOSH-I)
Inventor: IWAOKA T; KOBAYASHI M; KOYANO H; TAKAIWA K; TAKAYASU A; TATENO M; YOSHINO Y

Number of Countries: 002 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020167897 | A1 | 20021114 | US 20012741 | A | 20011115 | 200319 | B |
| JP 2002344465 | A | 20021129 | JP 2001143148 | A | 20010514 | 200319 | |

Priority Applications (No Type Date): JP 2001143148 A 20010514
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020167897 | A1 | | 27 | H04J-001/16 | |
| JP 2002344465 | A | | 18 | H04L-012/437 | |


Abstract (Basic): US 20020167897 A1

NOVELTY - A **clock** extractor (4-1) extracts transmission frequency **clock** in output signal of changeover switch (3-1), and outputs to a PLL circuit (4-2). On receiving output **clock** from the PLL circuit, a transmission frequency **clock** changing unit (5-1) reads out the stored output data of changeover switch, for performing a **clock** change and outputs to a frame generator (6). The frame generator frames the input **data based** on the **clock** input from the PLL circuit.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for node device comprising redundant changeover apparatus.

USE - For WDM based ring network, SONET/SDH transmission device.

ADVANTAGE - Achieves transparent transmission of any signals because of an **asynchronous** network, in which redundant changeover can be performed without **synchronization** loss spreading over network in its entirety. Eliminates frequent changing of frame format or transmission speed at the time of redundant changeover within transmission devices. Prevents frame **synchronization** loss from arising even upon changeover between working system and protection system.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of redundant changeover apparatus.

Changeover switch (3-1)
Frequency generator (4)
Transmission frequency **clock** extractor (4-1)
PLL circuit (4-2)
Frequency regenerator (5)
Transmission frequency **clock** changing unit (5-1)
Frame generator (6)
pp; 27 DwgNo 1/18

Title Terms: REDUNDANT; CHANGEOVER; APPARATUS; WDM; BASED; RING; NETWORK; FRAME; DATA; OUTPUT; THROUGH; CHANGEOVER; SWITCH; BASED; **CLOCK** ; SIGNAL; INPUT; PLL; CIRCUIT; RECEIVE; TRANSMISSION; FREQUENCY; **CLOCK** ; OUTPUT; SIGNAL; SWITCH
Derwent Class: U23; W01; W02
International Patent Class (Main): H04J-001/16; H04L-012/437
International Patent Class (Additional): H04B-010/02; H04L-007/033; H04L-012/43; H04Q-011/04
File Segment: EPI

19/5/2
DIALOG(R)File 350:Derwent WPIX


014911514 **Image available**
WPI Acc No: 2002-732220/200279
XRPX Acc No: N02-577369
**Application programming interface for network application, employs insertion and removal of pointer into data structures associated with operating system and network application for packet transmission and reception**
Patent Assignee: LUCENT TECHNOLOGIES INC (LUCE )
Inventor: BLOTT S; BRUSTOLONI J; MARTIN C E
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020138664 | A1 | 20020926 | US 2001815942 | A | 20010323 | 200279 | B |

Priority Applications (No Type Date): US 2001815942 A 20010323
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020138664 | A1 | | 14 | G06F-009/46 | |

Abstract (Basic): US 20020138664 A1
NOVELTY - Data packets to be transmitted from an operating system (OS) (102) are stored in a buffer and referred using pointers inserted by the OS into a source data structure (104A). The pointers are removed **asynchronously** by a network application (108) after reception. A target data structure (104B) is utilized during reception and the pointers inserted by the network application are removed by the OS, **asynchronously** .
USE - **Application programming interface** implemented on PC operating system for network application.
ADVANTAGE - By enabling **asynchronous** communication due to exchange of pointers to packets between the OS and the network application, system call overhead and risk of conflict between the OS and the application are avoided, thereby eliminating need for **synchronization** between them.
DESCRIPTION OF DRAWING(S) - The figure shows the schematic **application programming interface** .
Operating system (102)
Source data structure (104A)
Target data structure (104B)
Network application (108)
pp; 14 DwgNo 1/7
Title Terms: APPLY; PROGRAM; INTERFACE; NETWORK; APPLY; EMPLOY; INSERT; REMOVE; POINT; DATA; STRUCTURE; ASSOCIATE; OPERATE; SYSTEM; NETWORK; APPLY; PACKET; TRANSMISSION; RECEPTION
Derwent Class: T01
International Patent Class (Main): G06F-009/46
International Patent Class (Additional): G06F-015/16
File Segment: EPI

19/5/3
DIALOG(R)File 350:Derwent WPIX


014885404 **Image available**
WPI Acc No: 2002-706110/200276
XRPX Acc No: N02-556691
**SIM manager for GSM-type telephone SIM, initiates process thread relative to function call, and blocks further calls until selected function is complete**
Patent Assignee: MICROSOFT CORP (MICT ); SHEN A W (SHEN-I); VARGAS G R (VARG-I)
Inventor: SHEN A W; VARGAS G R

Number of Countries: 027 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| US 20020099871 | A1 | 20020725 | US 2001768587 | A | 20010125 | 200276 B |
| EP 1227397 | A2 | 20020731 | EP 2002960 | A | 20020116 | 200276 |

Priority Applications (No Type Date): US 2001768587 A 20010125
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020099871 | A1 | | 9 | G06F-009/46 | |
| EP 1227397 | A2 | E | | G06F-009/445 | |

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): US 20020099871 A1

NOVELTY - A dynamic link library (DLL) (204) is loaded by a stub dynamic link library (205), when stub DLL receives a call for performing a selected function from an application (201) operating in a GSM-type telephone device. The DLL initiates a process thread relative to the function call by activating communication between **API** corresponding to the function and radio interface layer (203), and blocks further calls until the selected function is completed.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Communication method for communication between **application** and radio **interface** layers within GSM-type telephone device; and

(2) Computer readable medium storing communication program.

USE - SIM manager for accessing functionalities such as phone book entries, passwords, files, stored messages, etc., within GSM-type telephone SIM card of hand-held device, multiprocessor system or programmable consumer electronic, network PC, minicomputer, mainframe computer, etc.

ADVANTAGE - Enables integration of several **asynchronous** radio interface larger (RIL) functions into single **synchronous API** , thereby allowing information to be safely read from or written to SIM card without possibility of another application invalidating the results. Enables removal of dynamic link library, when a cellular phone e.g. CDMA-type phone does not have a SIM card, thereby reducing ROM significantly.

DESCRIPTION OF DRAWING(S) - The figure shows the signal flow between selected layers of GSM-type telephone device.

Application (201)
Radio interface layer (203)
Dynamic link library (204,205)
pp; 9 DwgNo 2/2

Title Terms: MANAGE; TYPE; TELEPHONE; INITIATE; PROCESS; THREAD; RELATIVE; FUNCTION; CALL; BLOCK; CALL; SELECT; FUNCTION; COMPLETE
Derwent Class: T01; W01
International Patent Class (Main): G06F-009/445; G06F-009/46
International Patent Class (Additional): G06F-009/00
File Segment: EPI

**19/5/4**



014796707 **Image available**
WPI Acc No: 2002-617413/200266
XRPX Acc No: N02-488612

**Long term packet arrival rates measurement method for** asynchronous **transfer mode network, involves dividing counted known and predetermined samples with measured time** interval **of session**

Patent Assignee: PINES P J (PINE-I)
Inventor: PINES P J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|

US 20020078225 A1 20020620 US 2000229367 A 20000830 200266 B
US 2001943781 A 20010830

Priority Applications (No Type Date): US 2000229367 P 20000830; US 2001943781 A 20010830
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20020078225 A1 14 G06F-015/16 Provisional application US 2000229367

Abstract (Basic): US 20020078225 A1
NOVELTY - A known and predetermined number of data samples in a session are counted. A time **interval** between the initial and last data samples in the session are measured. A long term average arrival rate is calculated by dividing the counted samples with the measured time **interval** of the session.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) **Clock** rate **synchronization** method;
(2) Long term arrival rate measurement system;
(3) **Clock** rate **synchronization** system;
(4) Machine readable medium storing program for long term arrival rate measurement process; and
(5) Machine readable medium storing program for **synchronizing clock** rate of network.
USE - For measuring long term arrival rate of packets in **asynchronous** transfer mode (ATM) networks.
ADVANTAGE - Reduces or completely eliminates the quantization error as the counting of partial packets in the session is avoided. Improves the accuracy in calculating the average rate as the time **intervals** are accurately measured to very precise values.
DESCRIPTION OF DRAWING(S) - The figure shows a flowchart illustrating the long term arrival rate measurement process.
pp; 14 DwgNo 6/7
Title Terms: LONG; TERM; PACKET; ARRIVE; RATE; MEASURE; METHOD; **ASYNCHRONOUS** ; TRANSFER; MODE; NETWORK; DIVIDE; COUNT; PREDETERMINED; SAMPLE; MEASURE; TIME; **INTERVAL** ; SESSION
Derwent Class: T01; W01
International Patent Class (Main): G06F-015/16
File Segment: EPI

**19/5/5**
DIALOG(R)File 350:Derwent WPIX


014667141 **Image available**
WPI Acc No: 2002-487845/200252
Related WPI Acc No: 2002-279702
XRPX Acc No: N02-385473
**Flip-flop circuit used in Ethernet adapter for computer system, receives data signal coupled to logic devices connected to respective power supplies, for generating signal to be received by buffered keeper circuit**
Patent Assignee: INTEL CORP (ITLC )
Inventor: NARENDRA S; SACHDEV M
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 6369631 B1 20020409 US 2000608687 A 20000629 200252 B

Priority Applications (No Type Date): US 2000608687 A 20000629
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6369631 B1 9 H03K-003/356

Abstract (Basic): US 6369631 B1
NOVELTY - A multi-input conditional inverter (318) receives a data signal being coupled to pair of logic devices connected to respective power supplies and the control **clocks** , to generate a signal to be

received by a buffered keeper circuit.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Processing system;

(2) Computer readable medium storing data representing flip-flop circuit;

(3) Input signal latching method;

(4) Input signal latching apparatus; and

(5) Computer readable medium storing input signal latching program.

USE - Flip flop circuit for storage devices such as compact disk (CD)/digital versatile disk (DVD)/hard disk/optical disk drives, tape drive, flash, memory sticks, video recorders, etc., for displays such as cathode ray tube (CRT), liquid crystal display (LCD), a projection system, Television (TV), etc., for audio devices such as monophonic, stereo, three-dimensional sound card etc., for keyboard such as musical keyboard, keypad, series of switches etc for pointer such as mouse, touchpad, trackball, joystick etc., for input/output devices such as voice command input device, thumbprint device, smart card slot, personal computer (PC) card interface, virtual reality accessories etc., miscellaneous input/output devices such as musical instrument digital interface (MIDI) card etc., for communication device e.g. Ethernet adapter for local area network (LAN) connections, satellite connection, set-top box (STB) adapter, digital subscriber line adapter, wireless modem, telephone modem, direct telephone connection, hybrid fiber coax (HFC) connection, cable modem, etc., for mask programmable and flash type read only memory, static, dynamic, **synchronous** , **asynchronous** or any combination random access memory (RAM) for single, multiple or distributed central processing unit (CPU) in computer system (claimed).

ADVANTAGE - Because of reduced **clock** to output delay, the flip flops are extremely fast and the flip flops do not require any set up time.

DESCRIPTION OF DRAWING(S) - The figure shows a circuit diagram of the flip flop.

Multi-input conditional inverter (318)

pp; 9 DwgNo 3/6

Title Terms: FLIP; CIRCUIT; COMPUTER; SYSTEM; RECEIVE; DATA; SIGNAL; COUPLE ; LOGIC; DEVICE; CONNECT; RESPECTIVE; POWER; SUPPLY; GENERATE; SIGNAL; RECEIVE; BUFFER; KEEPER; CIRCUIT

Derwent Class: T01; U13; U21; U22

International Patent Class (Main): H03K-003/356

File Segment: EPI

**19/5/6**

DIALOG(R)File 350:Derwent WPIX



014586619 **Image available**

WPI Acc No: 2002-407323/200244

XRPX Acc No: N02-319893

**Agent interface device for television, includes timer which sets time for providing electronic program guide information to user, according to user preference**

Patent Assignee: SHARP KK (SHAF ); AOKI T (AOKI-I); INUI K (INUI-I); KESHI I (KESH-I); KUROMUSHA K (KURO-I); NAKAGAWA J (NAKA-I)

Inventor: AOKI T; INUI K; KESHI I; KUROMUSHA K; NAKAGAWA J

Number of Countries: 028 Number of Patents: 003

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 1189151 | A2 | 20020320 | EP 2001118605 | A | 20010802 | 200244 | B |
| US 20020059180 | A1 | 20020516 | US 2001908489 | A | 20010719 | 200244 | |
| JP 2002077755 | A | 20020315 | JP 2000258419 | A | 20000829 | 200244 | |

Priority Applications (No Type Date): JP 2000258419 A 20000829

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 1189151 | A2 | E | 26 | G06F-017/30 | |

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
US 20020059180 A1 G06F-007/00
JP 2002077755 A 13 H04N-005/44

Abstract (Basic): EP 1189151 A2

NOVELTY - An acquiring unit (106) acquires an electronic broadcast program guide. A preference database (108) analyzes the user preference from information provided by the acquiring unit and an **application program interface** (105). The analysis result is stored. An information providing engine (107) provides information to a user according to information stored in the preference **database** . A **timer** (112) sets the time of information provision.

USE - Agent interface device for home electronic apparatus such as TV, video recorder and optical disk player.

ADVANTAGE - The agent interface informs the user that the remaining capacity of the system resource is short for the current application, thus enables the user to take suitable measures to avoid the unstable operation of the system. User can operate variety of applications through interactions with the personified agent interface, hence the agent interface device can serve as a unified interface for variety of applications. And the user does not miss the chance of viewing a favorite television program, as the artificial agent displayed by the agent interface device previously informs about the broadcasting of the program. Detailed data related to the television program that the user has just viewed, can be obtained through the interaction with the agent interface. When the communication line of the agent interface device is connected to the Internet for a long period, the agent interface informs the user about the connection state, so as to enable the user to disconnect the connection.

DESCRIPTION OF DRAWING(S) - The figure shows a module of an agent interface device.

**Application program interface** (105)
Electronic broadcast program guide acquiring unit (106)
Information providing engine (107)
Preference database (108)
Timer (112)
pp; 26 DwgNo 2/21

Title Terms: AGENT; INTERFACE; DEVICE; TELEVISION; TIME; SET; TIME; ELECTRONIC; PROGRAM; GUIDE; INFORMATION; USER; ACCORD; USER; PREFER
Derwent Class: P86; T01; W03
International Patent Class (Main): G06F-007/00; G06F-017/30; H04N-005/44
International Patent Class (Additional): G06F-003/16; G06F-017/60; G10L-013/00; H04H-001/00
File Segment: EPI; EngPI

**19/5/7**
DIALOG(R)File 350:Derwent WPIX


014584385 **Image available**
WPI Acc No: 2002-405089/200243
XRPX Acc No: N02-318002

Timer **management system for data processing system, has** timer **services with handle function to output time-out message to user application or to application's task, on** timer **expiration**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); IBM UK LTD (IBMC )
Inventor: DAMON P; HEDDES M
Number of Countries: 096 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200227468 | A2 | 20020404 | WO 2001GB4322 | A | 20010927 | 200243 | B |
| AU 200190129 | A | 20020408 | AU 200190129 | A | 20010927 | 200252 | |

Priority Applications (No Type Date): US 2000675545 A 20000928
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|

WO 200227468 A2 E 24 G06F-009/00
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
AU 200190129 A G06F-009/00 Based on patent WO 200227468

Abstract (Basic): WO 200227468 A2

NOVELTY - An **API** (220) provides a set of **synchronous** functions that allows the user applications (210) to access **timer database** (230). **Timer** services (240) detects expiration of **timers** corresponding to each application that has initiated the **timer** via **API** , which has handle function to output a time-out message to user application or to application's task, on expiration, based on the type of utilized system, without incurring an illegal time-out messages.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) **Timer** management method in both **synchronous** and **asynchronous** system;

(b) Computer program for controlling data processing operation

USE - For managing **timers** in both **synchronous** and **asynchronous** data processing system.

ADVANTAGE - The handle function filters the illegal time-out messages by allowing the **asynchronous** application to **synchronously** act on the **timer** in the **asynchronous** system. The **timer** services detects the expiring of the **timers** in order to manage both single task system and multi-task system.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of a **timer** management system.

User application (210)
**API** (220)
**Timer database** (230)
**Timer** service (240)
pp; 24 DwgNo 2/4

Title Terms: TIME; MANAGEMENT; SYSTEM; DATA; PROCESS; SYSTEM; TIME; SERVICE ; HANDLE; FUNCTION; OUTPUT; TIME; MESSAGE; USER; APPLY; APPLY; TASK; TIME ; EXPIRE
Derwent Class: T01
International Patent Class (Main): G06F-009/00
File Segment: EPI

**19/5/8**
DIALOG(R)File 350:Derwent WPIX


014517533 **Image available**
WPI Acc No: 2002-338236/200237
Related WPI Acc No: 2000-328994; 2002-129585; 2002-722146
XRPX Acc No: N02-265853

**Dynamically tunable memory controller used in data processing system, controls delay between memory control operations to meet predetermined** timing **parameter**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: DELP G S; MCCLANNAHAN G P
Number of Countries: 001 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020013881 | A1 | 20020131 | US 98166004 | A | 19981002 | 200237 | B |
| | | | US 99247501 | A | 19990210 | | |
| | | | US 2001938161 | A | 20010823 | | |
| US 6453434 | B2 | 20020917 | US 98166004 | A | 19981002 | 200269 | |
| | | | US 99247501 | A | 19990210 | | |
| | | | US 2001938161 | A | 20010823 | | |

Priority Applications (No Type Date): US 99247501 A 19990210; US 98166004 A

19981002; US 2001938161 A 20010823
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020013881 | A1 | | 28 | G06F-012/00 | CIP of application US 98166004 |
| | | | | | Div ex application US 99247501 |
| US 6453434 | B2 | | | G11C-029/00 | CIP of application US 98166004 |
| | | | | | Div ex application US 99247501 |

Abstract (Basic): US 20020013881 A1

NOVELTY - A logic circuit (12) controls data transfer with memory by performing different memory control operations. A tuning circuit (22) is connected to the logic circuit for dynamically controlling delay between the memory control operations to meet predetermined **timing** parameter associated with **timing** characteristics selected from group containing bank cycle time, active command period time, precharge time.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Integrated circuit device;
(b) Data processing system;
(c) Program product for memory control;
(d) Data transfer control method;
(e) Circuit arrangement for use in determining optimum value from monotonically sorted list of values;
(f) Program product for determining optimum value from monotonically sorted list of values

USE - For dynamically tunable memory control e.g. for **synchronous** dynamic random access memory (SDRAM), enhanced **synchronous** DRAM, rambus DRAM, extended data out (EDO) DRAM, page mode DRAM, static RAM, flash memories, read only memories (ROM), electrically erasable programmable read only memory (EEPROM), serial EPROM, direct access storage device (DASD) subsystem implemented in integrated circuit (IC) device (claimed) used in data processing system (claimed) such as mid range computer system, e.g. AS/400 mid range computer, personal computer, main frame computer, super computer. Also in communication system such as bridge, router, switch, electronic devices. Also in network adaptor such as **asynchronous** transfer mode (ATM) adaptor, network adaptors for networks e.g. TCP/IP networks, LAN, WAN, frame relay networks.

ADVANTAGE - Utilizes tuning circuit that dynamically controls the **timing** of memory control operations rather than simply relying on fixed **timing** parameters, thereby determining optimum **timing** parameters without prior knowledge of performance characteristics of particular memory.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the memory controller.

Logic circuit (12)
Tuning circuit (22)
pp; 28 DwgNo 1/20

Title Terms: DYNAMIC; TUNE; MEMORY; CONTROL; DATA; PROCESS; SYSTEM; CONTROL ; DELAY; MEMORY; CONTROL; OPERATE; PREDETERMINED; TIME; PARAMETER
Derwent Class: T01
International Patent Class (Main): G06F-012/00; G11C-029/00
File Segment: EPI

**19/5/9**
DIALOG(R)File 350:Derwent WPIX


014482888 **Image available**
WPI Acc No: 2002-303591/200234
XRPX Acc No: N02-237569
**Workflow management method in enterprise, involves processing state transition process for process instance in** synchronous **or** asynchronous **mode based on predefined** synchronous **information**
Patent Assignee: HITACHI LTD (HITA ); BENIYAMA N (BENI-I); MATSUDA Y (MATS-I); SUZUKI A (SUZU-I)

Inventor: BENIYAMA N; MATSUDA Y; SUZUKI A
Number of Countries: 002 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020032692 | A1 | 20020314 | US 2001924505 | A | 20010809 | 200234 | B |
| JP 2002157386 | A | 20020531 | JP 2001220830 | A | 20010723 | 200239 | |

Priority Applications (No Type Date): JP 2000278673 A 20000908
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020032692 | A1 | | 44 | G06F-012/00 | |
| JP 2002157386 | A | | 25 | G06F-017/60 | |

Abstract (Basic): US 20020032692 A1

NOVELTY - A state transition for a process instance, is processed in **synchronous** mode during an **interval** of from accepting state transition request to receiving a response or in **asynchronous** mode after returning the response based on predefined **synchronous** information included in process definition.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Workflow management apparatus;

(b) Recorded medium storing workflow management program; Workflow management program

USE - For managing states of auxiliary work such as purchase activities and travel expense adjustment in enterprise and allocating the works to participants, for business activities such as window services.

ADVANTAGE - **Synchronous** information is referenced to determine whether processing for a state transition is to be performed in **synchronous** or **asynchronous** mode, thereby eliminating information related to methods of processing state transition request from source codes of workflow business processed programs. The workflow management system is flexible and sets simply amount of computer resource available for processing a state transition request depending on requirements of each activity or service.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the workflow management system.

pp; 44 DwgNo 1/35

Title Terms: MANAGEMENT; METHOD; PROCESS; STATE; TRANSITION; PROCESS; PROCESS; INSTANCE; **SYNCHRONOUS** ; **ASYNCHRONOUS** ; MODE; BASED; PREDEFINED ; **SYNCHRONOUS** ; INFORMATION
Derwent Class: T01
International Patent Class (Main): G06F-012/00; G06F-017/60
File Segment: EPI

**19/5/10**
DIALOG(R)File 350:Derwent WPIX


014149130 **Image available**
WPI Acc No: 2001-633349/200173
XRPX Acc No: N01-473192
**Multimedia network device generates suitable** clock **based on information indicating condition of communication path between auto-device and master network** synchronization **device**
Patent Assignee: FUJITSU LTD (FUIT )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 2001244918 | A | 20010907 | JP 200051508 | A | 20000228 | 200173 | B |

Priority Applications (No Type Date): JP 200051508 A 20000228
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 2001244918 | A | | 34 | H04L-007/00 | |

Abstract (Basic): JP 2001244918 A

NOVELTY - A master network **synchronization** device sends predefined initial values indicating condition of communication path between an auto-device and the master network **synchronization** device. A detector in a slave network **synchronization** device detects information related to normal communication path from the received values. Based on the detected information, suitable **clock** is generated by using **clock** determination **tables** (52-55).

USE - Multimedia network device with **clock** **synchronization** control function, by using **asynchronous** transfer mode (ATM) switching system.

ADVANTAGE - Improves **clock** generation accuracy, by considering condition of communication path between auto-device and master network **synchronization** device.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of network device. (Drawing includes non-English language text).

**Clock** determination **tables** (52-55)

pp; 34 DwgNo 1/22

Title Terms: NETWORK; DEVICE; GENERATE; SUIT; **CLOCK** ; BASED; INFORMATION; INDICATE; CONDITION; COMMUNICATE; PATH; AUTO; DEVICE; MASTER; NETWORK; DEVICE

Derwent Class: W01

International Patent Class (Main): H04L-007/00

International Patent Class (Additional): H04J-003/06; H04L-001/22; H04L-007/027; H04L-012/28

File Segment: EPI

**19/5/11**

DIALOG(R)File 350:Derwent WPIX



013991314 **Image available**

WPI Acc No: 2001-475529/200151

XRPX Acc No: N01-352032

**Client server based architecture for telecommunications network has IP which uses MCB as ATM fabric to communicate indirectly with MRM that provides gateway component for CPE management**

Patent Assignee: ADC TELECOM INC (ADCT-N)

Inventor: DIXON T J; ZIMMERMAN M

Number of Countries: 093 Number of Patents: 006

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200077990 | A1 | 20001221 | WO 2000US16390 | A | 20000614 | 200151 | B |
| AU 200058739 | A | 20010102 | AU 200058739 | A | 20000614 | 200151 | |
| EP 1190539 | A1 | 20020327 | EP 2000944678 | A | 20000614 | 200229 | |
| | | | WO 2000US16390 | A | 20000614 | | |
| BR 200011723 | A | 20020423 | BR 200011723 | A | 20000614 | 200235 | |
| | | | WO 2000US16390 | A | 20000614 | | |
| KR 2002015699 | A | 20020228 | KR 2001716206 | A | 20011217 | 200258 | |
| CN 1370362 | A | 20020918 | CN 2000811816 | A | 20000614 | 200303 | |

Priority Applications (No Type Date): US 99334431 A 19990616

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200077990 | A1 | E | 22 | H04L-012/64 | |

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW

| | | | | |
|---|---|---|---|---|
| AU 200058739 | A | | H04L-012/64 | Based on patent WO 200077990 |
| EP 1190539 | A1 | E | H04L-012/64 | Based on patent WO 200077990 |

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

| | | | | |
|---|---|---|---|---|
| BR 200011723 | A | | H04L-012/64 | Based on patent WO 200077990 |
| KR 2002015699 | A | | H04L-012/28 | |
| CN 1370362 | A | | H04L-012/64 | |

Abstract (Basic): WO 200077990 A1

NOVELTY - An Internet protocol (IP) module uses a multimedia channel bank (MCB) (320) as an **asynchronous** transfer mode (ATM) fabric to communicate indirectly with a multimedia resource manager (MRM) (330). The MRM provides a gateway component for a customer premises equipment (CPE) (340) management to separate application for e.g. configuration, alarms.

DETAILED DESCRIPTION - The IP module houses an IP processing e.g. routing, multi protocol label switching (MPLS). The IP module on the MCB terminates a physical drop in e.g. a **synchronous** digital subscriber line (SDSL) and maps an IP flow in to an ATM virtual circuit (VC). The IP processing, mapping profile, and the policing profile are dynamically enables by the MRM, upon triggers from the MCB. The MRM provides intelligence for an integrated access device (IAD) e.g. call agent.

USE - For telecommunications network.

ADVANTAGE - Allows intelligent allocation of bandwidth at MCB while keeping open environment for new enhancements. Provides mechanism for MCB to communicate with e.g. content provider, Internet service provider (ISP). Allows utilization of commercial database information models to tailor specific service or user profiles. Allows accessed network to respond to out of band control information and user requests on dedicated, specialized server platform. Allows network to handle e.g. protocols, **application** protocol **interface** ( **API** ) stacks. Has visibility to massive databases of service attributes, end-user profiles and accounts. Provides intelligence required to offer differentiated services on top of ATM/IP transport network.

DESCRIPTION OF DRAWING(S) - The figure shows a telecommunications network.

MCB (320)
MRM (330)
CPE (340)
pp; 22 DwgNo 3/4

Title Terms: CLIENT; SERVE; BASED; ARCHITECTURE; TELECOMMUNICATION; NETWORK ; IP; MCB; ATM; FABRIC; COMMUNICATE; INDIRECT; GATEWAY; COMPONENT; MANAGEMENT

Derwent Class: T01; W01

International Patent Class (Main): H04L-012/28; H04L-012/64

International Patent Class (Additional): H04Q-011/04

File Segment: EPI

**19/5/12**

DIALOG(R)File 350:Derwent WPIX



013605621 **Image available**

WPI Acc No: 2001-089829/200110

Related WPI Acc No: 2002-506633

XRPX Acc No: N01-067990

Asynchronous **transmit package buffer device for data communication system, reclaims memory containing transmitted portion of frame, for storage of new data prior to transmission completion**

Patent Assignee: 3COM CORP (THRE-N)

Inventor: HO N T; WANG C

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6128715 | A | 20001003 | US 97866822 | A | 19970530 | 200110 | B |

Priority Applications (No Type Date): US 97866822 A 19970530

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6128715 | A | | 14 | G06F-012/00 | |

Abstract (Basic): US 6128715 A

NOVELTY - The address pointers that are being read and written, are

**synchronized** simultaneously at the **clock** speeds. After transmission of first portion of a frame, the memory containing the first portion is reclaimed for storage of new data prior to frame transmission completion.

DETAILED DESCRIPTION - A bus interface (128) is coupled between dual ported memory (120) and host (110). Bus interface (126) is coupled between the memory and network (118). Both the bus interfaces comprised by logic device (124) have different **clocking** speeds. The logic device controls simultaneous transfer of frame data into or from the memory, at corresponding **clock** speeds. A **synchronization** interface coupled between the bus interfaces, **synchronizes** the address pointers. An INDEPENDENT CLAIM is also included for program product.

USE - For **asynchronous** transmit packet buffer for data communication system.

ADVANTAGE - The beginning of the frame can be downloaded while the end of the frame is still being constructed, reducing latency and improving efficiency of the entire host network system. Supports automatic reclaim of buffer space, unlimited burst transfer size and large packet transmission.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of network system.

Host (110)

Network (118)

Dual ported memory (120)

Bus interfaces (126,128)

pp; 14 DwgNo 1/7

Title Terms: **ASYNCHRONOUS** ; TRANSMIT; PACKAGE; BUFFER; DEVICE; DATA; COMMUNICATE; SYSTEM; RECLAIM; MEMORY; CONTAIN; TRANSMIT; PORTION; FRAME; STORAGE; NEW; DATA; PRIOR; TRANSMISSION; COMPLETE

Derwent Class: T01

International Patent Class (Main): G06F-012/00

File Segment: EPI

**19/5/13**

DIALOG(R)File 350:Derwent WPIX



013465262 **Image available**

WPI Acc No: 2000-637205/200061

XRPX Acc No: N00-472503

**Output controlling method of FIFO memory, involves monitoring period between write operation into memory and are processed to develop estimated ratio of local sample rate to rate of write operation**

Patent Assignee: CREATIVE TECHNOLOGY LTD (CREA-N)

Inventor: ROSSUM D P

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6092126 | A | 20000718 | US 97969312 | A | 19971113 | 200061 | B |

Priority Applications (No Type Date): US 97969312 A 19971113

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6092126 | A | | 14 | G06F-013/00 | |

Abstract (Basic): US 6092126 A

NOVELTY - Position of current read address is monitored relative to current write address of FIFO memory. The addresses are advanced along preset direction during corresponding read and write. The period between write operation is monitored and processed for estimate ratio of local sample rate to a rate of write operation. A set of operation corresponding to tracking mode is performed based on monitored position.

DETAILED DESCRIPTION - A primary tracking mode is selected when the monitored position indicates FIFO memory is full or empty. The corresponding set of operation include pre-biasing estimated ratio to accelerate movement of monitored position towards the center position

between full and empty. The second tracking mode includes filtering the estimated ratio. INDEPENDENT CLAIMS are also included for the following:

(a) apparatus for controlling output from FIFO memory;

(b) computer program product

USE - For controlling output of FIFO memory **synchronous** to local **clock** in CD player, DAT player, DVD player and web sites having audio materials.

ADVANTAGE - The tracking loops control the FIFO memory to provide rapid acquisition and good steady state performance. One tracking loop is used for rapid acquisition, when the buffer is either empty or full. Another tracking loop incorporates a low pass filter to remove the effects of momentary variations in input sampling rates and used for steady state operation.

DESCRIPTION OF DRAWING(S) - The figure shows the process of filtering applied to input sampling frequency in **asynchronous** sample rate converter.

pp; 14 DwgNo 3/6

Title Terms: OUTPUT; CONTROL; METHOD; FIFO; MEMORY; MONITOR; PERIOD; WRITING; OPERATE; MEMORY; PROCESS; DEVELOP; ESTIMATE; RATIO; LOCAL; SAMPLE; RATE; RATE; WRITING; OPERATE

Derwent Class: T01

International Patent Class (Main): G06F-013/00

File Segment: EPI

**19/5/14**

DIALOG(R)File 350:Derwent WPIX



013422173 **Image available**

WPI Acc No: 2000-594113/200056

XRPX Acc No: N00-440039

**Digital telephone for telephone communication system has PBX connected to server and PC which provides user with all functions of phone on the PC**

Patent Assignee: VOICE TECHNOLOGIES GROUP INC (VOIC-N); DIALOGIC INC (DIAL-N)

Inventor: DYLAG E M; FRITZINGER R

Number of Countries: 090 Number of Patents: 005

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200051299 | A1 | 20000831 | WO 2000US5037 | A | 20000225 | 200056 | B |
| AU 200033830 | A | 20000914 | AU 200033830 | A | 20000225 | 200063 | |
| EP 1157510 | A1 | 20011128 | EP 2000912030 | A | 20000225 | 200201 | |
| | | | WO 2000US5037 | A | 20000225 | | |
| JP 2002538667 | W | 20021112 | JP 2000601795 | A | 20000225 | 200275 | |
| | | | WO 2000US5037 | A | 20000225 | | |
| CN 1375145 | A | 20021016 | CN 2000806840 | A | 20000225 | 200311 | |

Priority Applications (No Type Date): US 99121755 P 19990226

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200051299 | A1 | E | 47 | H04L-012/66 | |

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW

| | | | | | |
|---|---|---|---|---|---|
| AU 200033830 | A | | | H04L-012/66 | Based on patent WO 200051299 |
| EP 1157510 | A1 | E | | H04L-012/66 | Based on patent WO 200051299 |

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

| | | | | | |
|---|---|---|---|---|---|
| JP 2002538667 | W | | 39 | H04L-012/66 | Based on patent WO 200051299 |
| CN 1375145 | A | | | H04L-012/66 | |

Abstract (Basic): WO 200051299 A1

NOVELTY - PBX (12) is connected through a computer telephony server

(30) to a personal computer (20) which is connected through standard interface lines (14,16) to digital telephone. Communication link (32) such as LAN, WAN, RAS, internet are connected to server and PC. Phone server includes a digital phone emulation interface (34), an apllication **program interface** (36) and logic (38).

DETAILED DESCRIPTION - Interface provides a direct digital connection between PBX and PC. **Application program interface** develops a command set from signals provided by interface which the software in PC can understand. Logic serves as an intermediary between **synchronous** switching on the PBX side of the server and **asynchronous** packet switching on the PC side of the server.

AN INDEPENDENT CLAIM is also included for method of performing key press transaction in telephone communication system.

USE - Telephone communication system for performing all function of telephone on a PC.

ADVANTAGE - Computer cab be access to utilize the digital telephone functions from a remote location with communication via internet, LAN, WAN, RAS or other mediums.

DESCRIPTION OF DRAWING(S) - Drawing shows a block diagram of the system.

PBX (12)
Standard interface lines (14,16)
Personal computer (20)
Computer telephony server (30)
Communication link (32)
Interface (34)
Apllication **program interface** (36)
Logic (38)
pp; 47 DwgNo 1/9

Title Terms: DIGITAL; TELEPHONE; TELEPHONE; COMMUNICATE; SYSTEM; PBX; CONNECT; SERVE; USER; FUNCTION; TELEPHONE
Derwent Class: W01
International Patent Class (Main): H04L-012/66
International Patent Class (Additional): G06F-003/00; H04M-011/00
File Segment: EPI

**19/5/15**

DIALOG(R)File 350:Derwent WPIX


013319753 **Image available**
WPI Acc No: 2000-491691/200044
XRAM Acc No: C00-147909
XRPX Acc No: N00-364828

**Control of twin, geared electric motor drives of withdrawal conveyor serving plastic profile extrusion plant, employs programmable system of frequency converters sensing and correcting differential speed and torque**

Patent Assignee: SEW-EURODRIVE GMBH & CO (SEWE-N)
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| DE 19859348 | A1 | 20000706 | DE 1059348 | A | 19981222 | 200044 | B |

Priority Applications (No Type Date): DE 1059348 A 19981222
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| DE 19859348 | A1 | | 10 | G05B-013/00 | |

Abstract (Basic): DE 19859348 A1

NOVELTY - Each drive employs a preferably geared electric motor, an angular sensor and a frequency converter with control software. The frequency converter casing includes configurable and/or freely **programmable** control, with **interfaces** exchanging data. Connections, construction and motor control assure identical withdrawal conveyor speeds.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for corresponding control equipment. Preferred features: **Synchronous** or

**asynchronous** motors are employed. Software control is provided with includes suitable I/O interfacing. One drive operates as master, the other as slave, the former sending data to and/or receiving it from the latter. They operate under speed control. Programmable control of the slave drive frequency converter, varies torque or current vector to achieve required slave speed. A control algorithm, based on a proportionality factor operating on the differential torque between slave and master, is employed. An alternative algorithm is proposed. Further variants based on the foregoing principles are described. Limiters and proportionality factor adjustments are included.

USE - To control speed of withdrawal conveyors serving a plastic section extrusion machine.

ADVANTAGE - The economical drive control system overcomes problems, e.g. of wear and lengthening of the withdrawal chains, which arises over a protracted interval. These and other defects, cause operation at differing speeds in prior art. The new control system also avoids any transverse component of force on the product, preventing distortion. No slippage emerges between chain and product, and there is no drive fluctuation, either of which can detract from product quality.

DESCRIPTION OF DRAWING(S) - The sketch gives a general impression of the withdrawal system.

pp; 10 DwgNo 1/4

Title Terms: CONTROL; TWIN; GEAR; ELECTRIC; MOTOR; DRIVE; WITHDRAW; CONVEYOR; SERVE; PLASTIC; PROFILE; EXTRUDE; PLANT; EMPLOY; PROGRAM; SYSTEM; FREQUENCY; CONVERTER; SENSE; CORRECT; DIFFERENTIAL; SPEED; TORQUE

Derwent Class: A32; T06; V06; X13; X25

International Patent Class (Main): G05B-013/00

International Patent Class (Additional): B29C-047/92; H02P-005/46

File Segment: CPI; EPI

**19/5/16**

DIALOG(R)File 350:Derwent WPIX



013241526 **Image available**

WPI Acc No: 2000-413408/200036

XRAM Acc No: C00-125377

XRPX Acc No: N00-308748

**Control method for extrusion machine with twin tracked caterpillar take-off whose drive units include motors and frequency converters giving identical track speeds**

Patent Assignee: SEW-EURODRIVE GMBH & CO (SEWE-N)

Inventor: SCHAEFFER R; STENKAMP D

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| DE 19851531 | A1 | 20000608 | DE 1051531 | A | 19981109 | 200036 | B |

Priority Applications (No Type Date): DE 1051531 A 19981109

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| DE 19851531 | A1 | | 6 | B65G-043/00 | |

Abstract (Basic): DE 19851531 A1

NOVELTY - The drive units (1,2) power the caterpillar tracks through pinions and comprise geared electric motors with an angle sensor (4,5) and a frequency converter with an integrated **programmable** control and **interface** points for data exchange. The frequency converters are electrically connected and the motors (M) can be controlled to ensure equal speeds on the take-off tracks.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is made for an extrusion machine with a product take-off unit which employs the claimed control method.

USE - For controlling the speed of tracks on a extrusion machine take-off unit, e.g. for plastic profile production.

ADVANTAGE - Speed variation in each track is avoided giving a product surface with no obvious waviness and the take-off tracks have a

longer life.
DESCRIPTION OF DRAWING(S) - The drawing shows the control process.
master drive unit (1)
slave drive unit (2)
angle sensor (4,5)
motor (M)
pp; 6 DwgNo 2/2
Title Terms: CONTROL; METHOD; EXTRUDE; MACHINE; TWIN; TRACK; DRIVE; UNIT; MOTOR; FREQUENCY; CONVERTER; IDENTICAL; TRACK; SPEED
Derwent Class: A32; A93; Q35; T06; X13; X25
International Patent Class (Main): B65G-043/00
International Patent Class (Additional): B29C-047/92; B65G-015/14; G05B-019/02; H02P-007/67
File Segment: CPI; EPI; EngPI

**19/5/17**
DIALOG(R)File 350:Derwent WPIX


012979735 **Image available**
WPI Acc No: 2000-151588/200014
XRPX Acc No: N00-112574
Asynchronous **data-reading apparatus**
Patent Assignee: NEC CORP (NIDE ); NEC SHIZUOKA LTD (NIDE )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 2000010951 | A | 20000114 | JP 98187011 | A | 1998061 | 200014 | B |

Priority Applications (No Type Date): JP 98187011 A 19980618
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 2000010951 | A | | 5 | G06F-015/177 | |

Abstract (Basic): JP 2000010951 A
NOVELTY - A latch **clock** generator (4) produces a **clock** which **synchronized** with **asynchronous** data. A latching circuit (6) latches **asynchronous** data, **synchronizing** with the generated **clock** . When a latch stop-signal generator (3) is stopping the generated **clock** , a multiprocessor device (1) reads out the **asynchronous** data latched with the latching circuit.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) an **asynchronous** data-reading procedure;
(b) and a recording medium.
USE - None given.
ADVANTAGE - Stable **asynchronous** data can be read out by performing read-out **synchronizing** with **clock** .
DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the **asynchronous** -data reading apparatus.
Multiprocessor device (1)
Latch stop-signal generator (3)
Latch **clock** generator (4)
Latching circuit (6)
pp; 5 DwgNo 1/2
Title Terms: **ASYNCHRONOUS** ; DATA; READ; APPARATUS
Derwent Class: T01
International Patent Class (Main): G06F-015/177
International Patent Class (Additional): H04L-007/00
File Segment: EPI

**19/5/18**
DIALOG(R)File 350:Derwent WPIX


012888233 **Image available**

WPI Acc No: 2000-060067/200005
XRPX Acc No: N00-428833

Asynchronous **communication data calling and incoming call signaling servicing method, involves servicing subscriber with** asynchronous **communication data after data terminal receives connect modem response message**

Patent Assignee: KOREA ELECTRONICS & TELECOM RES INST (KOEL-N); KOREA ELECTRONICS & TELECOM RES (KOEL-N); ELECTRONICS & TELECOM RES INST (ELTE-N)
Inventor: BAIK I K; JANG S H; KWEON H Y; BAEK I G; CHANG S H; KWON H Y

Number of Countries: 002 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| KR 98080470 | A | 19981125 | KR 989536 | A | 19980319 | 200005 | B |
| US 6111866 | A | 20000829 | US 9850978 | A | 19980331 | 200055 | |
| KR 260516 | B1 | 20000701 | KR 989536 | A | 19980319 | 200131 | |

Priority Applications (No Type Date): KR 9711987 A 19970401
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| KR 98080470 | A | | | H04B-001/69 | |
| US 6111866 | A | | 9 | H04J-013/00 | |
| KR 260516 | B1 | | | H04B-001/69 | |

Abstract (Basic): US 6111866 A

NOVELTY - The CDMA network receives modem initialization commands and modem dial command for modem control. A data terminal receives a connect modem response message informing a call connection with the counterpart, from the IWF of CDMA network. A subscriber is serviced with **asynchronous** communication data after data terminal has received the response message.

DETAILED DESCRIPTION - The subscriber attempts a call with modem dial command in case where the configuration of mobile station which the mobile subscriber has, is a data terminal and a mobile terminal. The data terminal recognizes the modem dial command and sends a call origination signal to the mobile terminal. The mobile terminal initiates a data call following the same call processing as that of a voice. The mobile terminal and CDMA network concurrently initialize radio link protocol, when a traffic channel is allocated from the base station to the mobile terminal and a service option is responded. The point-to-point protocols of the data terminal and a IWF of the CDMA network are self initialized after the data terminal receives the modem connection confirmation signal. A link control protocol is driven so as to initiate and **synchronize** a serial link after point-to-point protocols are self-initiated. The transmission control protocol/Internet protocol are driven after the transmission control protocol/Internet protocol are initiated and an address is allocated to the internet protocol. The **application interface** of the data terminal sends according to the transmission control protocol/Internet protocol modem initialization commands and modem dial command for modem control to the IWF of the CDMA network.

USE - For data servicing in CDMA mobile communication network.

ADVANTAGE - Since interworking function is provided, the reliability of the wireless communication environment is not lowered due to noise, fading and handover etc.

DESCRIPTION OF DRAWING(S) - The figure shows the flow diagram explaining data service incoming call procedure and protocol operation.

pp; 9 DwgNo 6/6

Title Terms: **ASYNCHRONOUS** ; COMMUNICATE; DATA; CALL; INCOMING; CALL; SERVICE; METHOD; SERVICE; SUBSCRIBER; **ASYNCHRONOUS** ; COMMUNICATE; DATA; AFTER; DATA; TERMINAL; RECEIVE; CONNECT; MODEM; RESPOND; MESSAGE

Derwent Class: W01; W02
International Patent Class (Main): H04B-001/69; H04J-013/00
International Patent Class (Additional): H04Q-007/00
File Segment: EPI

19/5/19
DIALOG(R)File 350:Derwent WPIX


012721011 **Image available**
WPI Acc No: 1999-527123/199944
XRPX Acc No: N99-390453
Synchronous **pipelined static random access memory (SRAM) circuitry with** programmable **scan** interface
Patent Assignee: CYPRESS SEMICONDUCTOR CORP (CYPR-N)
Inventor: CHURCHILL J F; FINN M A; PANCHOLY A; PHELAN C G; RAFTERY N P; SHANMUGAM J; SURRETTE T M
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5953285 | A | 19990914 | US 97932638 | A | 19970917 | 199944 | B |

Priority Applications (No Type Date): US 97932638 A 19970917
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5953285 | A | | 28 | G11C-008/00 | |

Abstract (Basic): US 5953285 A
NOVELTY - An output register (208) receives a register input and outputs a **synchronous** mode and an **asynchronous** mode of operation. A **programmable** scan **interface** (212) is coupled to the output register to control whether the register operates in the **synchronous** mode or the **asynchronous** mode.
USE - None given.
ADVANTAGE - Improves memory core operation without any undesirable output register masking effects since the data flow through the register is monitored.
DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the **synchronous** pipelined SRAM including the **programmable** scan **interface** .
Output register (208)
**Programmable** scan **interface** (212)
pp; 28 DwgNo 2/14
Title Terms: **SYNCHRONOUS** ; PIPE; STATIC; RANDOM; ACCESS; MEMORY; SRAM; CIRCUIT; PROGRAM; SCAN; INTERFACE
Derwent Class: U13; U14
International Patent Class (Main): G11C-008/00
File Segment: EPI

19/5/20
DIALOG(R)File 350:Derwent WPIX


012519723 **Image available**
WPI Acc No: 1999-325829/199927
XRPX Acc No: N99-244342
**Interactive viewing system for linking video services and in television systems**
Patent Assignee: MICROSOFT CORP (MICR-N)
Inventor: MATTHEWS J H; SHOFF D J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5900905 | A | 19990504 | US 96657566 | A | 19960605 | 199927 | B |

Priority Applications (No Type Date): US 96657566 A 19960605
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5900905 | A | | 18 | H04N-007/14 | |

Abstract (Basic): US 5900905 A
NOVELTY - A **controller** is adapted to transfer script database and

bitmaps between two memories and to interpret and display script database to determine video segment to be displayed on the video display. The **controller** responds to command input via an input device, launches application associated with video segment and transfers title of video segment.

DETAILED DESCRIPTION - The system has a head end in the two way communication system with viewer stations having video display coupled to **controller** and input device. The head end has a memory for storing script database which gives the order of video segments to be displayed. The **controller** has another memory for storing transferred script database. The script database is hierarchical **database** including **timing** information related to length of video segment.

USE - For linking video services, television systems, market research, polling, noting, promoting programs on channels.

ADVANTAGE - User can immediately respond to informational messages without need for another communication medium such as telephone or mail service.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart of interactive information system showing sequence through video segments including **initialization** .

pp; 18 DwgNo 5/7

Title Terms: INTERACT; VIEW; SYSTEM; LINK; VIDEO; SERVICE; TELEVISION; SYSTEM

Derwent Class: T01; T05; W01; W02

International Patent Class (Main): H04N-007/14

File Segment: EPI

**19/5/21**

DIALOG(R)File 350:Derwent WPIX



012437332 **Image available**

WPI Acc No: 1999-243440/199920

XRPX Acc No: N99-181177

Asynchronous **digital testing module for integrated circuit**

Patent Assignee: CYPRESS SEMICONDUCTOR CORP (CYPR-N)

Inventor: CHAN E

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5889936 | A | 19990330 | US 95561886 | A | 19951122 | 199920 | B |

Priority Applications (No Type Date): US 95561886 A 19951122

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5889936 | A | | 14 | G06F-011/08 | |

Abstract (Basic): US 5889936 A

NOVELTY - A serial-parallel converter (332) receives a first **clock** signal and serial stream of output test data by **clocking** in the test **data based** on the first **clock** signal and converts the serial stream of output test data into parallel output test data. A FIFO memory (333) is coupled to receive the second **clock** signal and parallel output test data in response to second **clock** signal.

DETAILED DESCRIPTION - A phase locked loop (331) coupled to a device (320) under test, receives a serial stream of output test data from the device and generates first and second **clock** signals. The first and second **clock** signals are generated independent of whether the serial stream of output test data is **synchronous** or **asynchronous** .

The serial-parallel converter comprises several D flip-flops coupled in series. The parallel output test data includes multiple output test vectors each having corresponding input test vector.

USE - For high speed functional testing of integrated circuit.

ADVANTAGE - Performs complete functional testing of device operating under real time operating condition or at very fast speeds. Uses computer to determine whether the device generates correct output

test data for each test procedure. Simplifies control and **clock** distribution scheme, thus storing input or output test data in memory device, efficiently.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of a digital testing module.

Device (320)

Phase locked loop (331)

Serial-parallel converter (332)

FIFO memory (333)

pp; 14 DwgNo 3/7

Title Terms: **ASYNCHRONOUS** ; DIGITAL; TEST; MODULE; INTEGRATE; CIRCUIT
Derwent Class: S01; T01; U11
International Patent Class (Main): G06F-011/08
File Segment: EPI

**19/5/22**

DIALOG(R)File 350:Derwent WPIX


012415248 **Image available**
WPI Acc No: 1999-221356/199919
XRPX Acc No: N99-164193

**Digital communication apparatus for data decoding and encoding of data - has frequency divider for generating** clock **signal which is** synchronized **to remove noise from input** asynchronous data , based **on which** timing **signal is generated for data encoding**

Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 11055235 | A | 19990226 | JP 97208786 | A | 19970804 | 199919 | B |

Priority Applications (No Type Date): JP 97208786 A 19970804
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 11055235 | A | | 9 | H04L-007/04 | |

Abstract (Basic): JP 11055235 A

NOVELTY - The symbol circuit has a frequency divider (17) for generating a **clock** pulse (18) which is **synchronized** to remove noise from input **asynchronous** data (19). A noise filter (20) generates a **timing** signal (34) for data encoding, based on delay signal (29). The encoding of the noiseless **asynchronous** data is done by **synchronizing** the **timing** signal with the **clock** pulse.

USE - For encoding and decoding of data.

ADVANTAGE - The encoding and decoding of data by the removal of noise is made highly reliable by **synchronizing** the few sample **clock** pulse at high speed. DESCRIPTION OF DRAWING(S) - The drawing shows the block diagram of the digital communication apparatus. (17) Frequency divider; (18) **Clock** pulse; (19) **Asynchronous** data; (20) Noise filter; (29) Delay signal; (34) **Timing** signal.

Dwg.1/8

Title Terms: DIGITAL; COMMUNICATE; APPARATUS; DATA; DECODE; ENCODE; DATA; FREQUENCY; DIVIDE; GENERATE; **CLOCK** ; SIGNAL; REMOVE; NOISE; INPUT; **ASYNCHRONOUS** ; DATA; BASED; TIME; SIGNAL; GENERATE; DATA; ENCODE
Derwent Class: W01
International Patent Class (Main): H04L-007/04
File Segment: EPI

**19/5/23**

DIALOG(R)File 350:Derwent WPIX


011638380 **Image available**
WPI Acc No: 1998-055288/199806
XRPX Acc No: N98-043792

**Object oriented computer system** programmer interface **- has at least one dynamic slot which provides** asynchronous **execution of programmer submitted functions and also at least one** synchronous **and** asynchronous **slot**

Patent Assignee: SIEMENS AG (SIEI )
Inventor: BECKER D; DORN K; QUEHL D
Number of Countries: 020 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 817018 | A2 | 19980107 | EP 97110676 | A | 19970630 | 199806 | B |
| JP 10124330 | A | 19980515 | JP 97178313 | A | 19970703 | 199830 | |
| US 6012081 | A | 20000104 | US 96675616 | A | 19960703 | 200008 | |

Priority Applications (No Type Date): US 96675616 A 19960703
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 817018 | A2 | E | 33 | G06F-009/46 | |
| | Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE | | | | |
| JP 10124330 | A | | 23 | G06F-009/46 | |
| US 6012081 | A | | | G06F-009/00 | |

Abstract (Basic): EP 817018 A

The object oriented computing system **programmer interface** system on a computer platform includes at least one dynamic slot which provides **asynchronous** execution of programmer submitted functions. There is at least one **synchronous** timer slot and at least one **asynchronous** timer slot. There is at least one exception slot for handling programmer defined system exception callbacks and at least one slot providing external event notification for programmer events.

There is a thread dispatcher, a main dispatcher and a signalling dispatcher. A thread manager controls execution of threads required by a slot. A message block memory stores message blocks. A list of activity identifiers return an error external event notification for user events. An administrator maps the activity identifiers to slot identifiers. A queue is provided for blocked threads.

ADVANTAGE - Provides operating system independent high level framework. Provides usage of threads for **asynchrony** and independence from operating systems which do not support **asynchrony** . Supports very high level wait for event interface which allows single high level applications mainloop to capture all low level operating system dependent event dispatching as well as high level application event dispatching.

Dwg.1/23

Title Terms: OBJECT; ORIENT; COMPUTER; SYSTEM; PROGRAM; INTERFACE; ONE; DYNAMIC; SLOT; ,**ASYNCHRONOUS** ; EXECUTE; PROGRAM; SUBMIT; FUNCTION; ONE; **SYNCHRONOUS** ; **ASYNCHRONOUS** ; SLOT
Derwent Class: T01
International Patent Class (Main): G06F-009/00; G06F-009/46
File Segment: EPI

**19/5/24**



011562826 **Image available**
WPI Acc No: 1997-539307/199750
XRPX Acc No: N97-448868

**Data communication server system for communication network - has device responsive to receipt of reply to** asynchronous **communication associates reply with request from client system to enable reply to be sent to client system**

Patent Assignee: IBM CORP (IBMC ); INT BUSINESS MACHINES CORP (IBMC ); IBM UK LTD (IBMC )
Inventor: NIBLETT P D; RANDELL K L
Number of Countries: 026 Number of Patents: 010
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| GB 2313524 | A | 19971126 | GB 9610898 | A | 19960524 | 199750 | B |
| WO 9745798 | A1 | 19971204 | WO 97GB1384 | A | 19970519 | 199803 | |
| CN 1219257 | A | 19990609 | CN 97194785 | A | 19970519 | 199941 | |
| JP 11510632 | W | 19990914 | JP 97541809 | A | 19970519 | 199948 | |
| | | | WO 97GB1384 | A | 19970519 | | |
| CZ 9803811 | A3 | 19991013 | WO 97GB1384 | A | 19970519 | 199949 | |
| | | | CZ 983811 | A | 19970519 | | |
| HU 9902190 | A2 | 19991129 | WO 97GB1384 | A | 19970519 | 200003 | |
| | | | HU 992190 | A | 19970519 | | |
| EP 978056 | A1 | 20000209 | EP 97923216 | A | 19970519 | 200012 | |
| | | | WO 97GB1384 | A | 19970519 | | |
| KR 2000010691 | A | 20000225 | WO 97GB1384 | A | 19970519 | 200102 | |
| | | | KR 98708764 | A | 19981030 | | |
| KR 275403 | B | 20001215 | WO 97GB1384 | A | 19970519 | 200175 | |
| | | | KR 98708764 | A | 19981030 | | |
| US 6336135 | B1 | 20020101 | WO 97GB1384 | A | 19970519 | 200207 | |
| | | | US 98180986 | A | 19981119 | | |

Priority Applications (No Type Date): GB 9610898 A 19960524

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| GB 2313524 | A | | 36 | H04L-012/66 | |
| WO 9745798 | A1 | E | 34 | G06F-017/30 | |
| Designated States (National): CN CZ HU JP KR PL RU US | | | | | |
| Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE | | | | | |
| CN 1219257 | A | | | G06F-017/30 | |
| JP 11510632 | W | | 50 | G06F-015/00 | Based on patent WO 9745798 |
| CZ 9803811 | A3 | | | G06F-017/30 | Based on patent WO 9745798 |
| HU 9902190 | A2 | | | G06F-017/30 | Based on patent WO 9745798 |
| EP 978056 | A1 | E | | G06F-017/30 | Based on patent WO 9745798 |
| Designated States (Regional): BE CH DE ES FR GB IE IT LI NL SE | | | | | |
| KR 2000010691 | A | | | G06F-015/173 | Based on patent WO 9745798 |
| KR 275403 | B | | | G06F-015/173 | Previous Publ. patent KR 2000010691<br>Based on patent WO 9745798 |
| US 6336135 | B1 | | | G06F-015/16 | Based on patent WO 9745798 |

Abstract (Basic): GB 2313524 A

The system includes a device, responsive to a request from a client system within a **synchronous** communication session between the client system and a server system (230), for sending a request to a program on the server system or on another system of the network as an **asynchronous** communication. A device responsive to receipt of a reply to the **asynchronous** communication associates the reply with the request from the client system to enable a reply to be sent to the client system. A device generates a preliminary reply before receipt of a reply to the **asynchronous** communication.

A gateway **program** (200) **interfaces** between message queue manager program (210) and a Web server program (220) installed on computer system. The application program is able to interpret HTML from data from Web Browser (250).

USE/ADVANTAGE - For providing links between different communication environments. Allows to operate seamlessly and without user knowledge of complexities of interaction. Provides link between different resources.

Dwg.3/5

Title Terms: DATA; COMMUNICATE; SERVE; SYSTEM; COMMUNICATE; NETWORK; DEVICE ; RESPOND; RECEIPT; REPLY; **ASYNCHRONOUS** ; COMMUNICATE; ASSOCIATE; REPLY; REQUEST; CLIENT; SYSTEM; ENABLE; REPLY; SEND; CLIENT; SYSTEM

Derwent Class: T01

International Patent Class (Main): G06F-015/00; G06F-015/16; G06F-015/173; G06F-017/30; H04L-012/66

International Patent Class (Additional): G06F-009/46; G06F-013/00; G06F-015/163; H04L-029/06; H04L-029/08

File Segment: EPI

19/5/25
DIALOG(R)File 350:Derwent WPIX


011385938 **Image available**
WPI Acc No: 1997-363845/199733
XRPX Acc No: N97-302441
**System for transferring messages between applications in distributed environments - has regions executing different applications, with associated messaging interface creating communication session between applications**
Patent Assignee: MCI COMMUNICATIONS CORP (MCIC-N)
Inventor: HOLMES R K; KRUEGER K C
Number of Countries: 020 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 9724664 | A1 | 19970710 | WO 96US20342 | A | 19961227 | 199733 | B |

Priority Applications (No Type Date): US 95580950 A 19951229
Cited Patents: 1.Jnl.Ref; EP 539130; EP 600235
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 9724664 | A1 | E | 29 | G06F-009/46 | |

Designated States (National): CA JP MX
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Abstract (Basic): WO 9724664 A
The system includes a data processing system divided into regions which execute different applications, and a messaging interface associated with each application for creating a communication session between the applications. An **application program interface** is invoked by an application call.
A configuration file in response to a call parameter provides the address of an application to be connected to a session, and a protocol in which to conduct the session. A repository stores and forwards a message to the application to be connected. A communication transport mechanism establishes a session with the application to be connected using the obtained protocol and destination and forwards the message to the application concerned.
ADVANTAGE - Allows **synchronous** and **asynchronous** communication between application programs running in distributed computing environment.
Dwg.1/4
Title Terms: SYSTEM; TRANSFER; MESSAGE; APPLY; DISTRIBUTE; ENVIRONMENT; REGION; EXECUTE; APPLY; ASSOCIATE; INTERFACE; COMMUNICATE; SESSION; APPLY
Derwent Class: T01; W01
International Patent Class (Main): G06F-009/46
File Segment: EPI

19/5/26
DIALOG(R)File 350:Derwent WPIX


011212684 **Image available**
WPI Acc No: 1997-190609/199717
XRPX Acc No: N97-157609
**Data substitution method for data transmission system in** synchronous **and** asynchronous **data networks - involves correcting error of transferred data by subtracting computed correction value from numerical value of transmitted data**
Patent Assignee: FUJITSU LTD (FUIT )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 9051362 | A | 19970218 | JP 95199572 | A | 19950804 | 199717 | B |

Priority Applications (No Type Date): JP 95199572 A 19950804
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 9051362 | A | | 22 | H04L-029/02 | |

Abstract (Basic): JP 9051362 A

The method involves supervision of the phase difference between the input and output data by a phase difference monitoring module (1). A **timing** selector (2) determines the switching **timing** of the output **data based** on the phase difference output by the phase difference monitoring module. A data monitoring module (3) keeps track of the numerical value of the data transferred from the input module to the output module. A total error computation module calculates the cumulative error which occurs during data transfer.

An error memory stores the total error value temporarily. A correction value computation module calculates the correction value based on stored total error value and the data output by data monitoring module. All the modules together with an error correction range controller constitute an error state monitoring module (4). The error correction value is subtracted from the numerical value of data by an error correction module (5).

ADVANTAGE - Blocks transmission of generated phase error to output module. Improves quality of data transmission.

Dwg.1/18

Title Terms: DATA; SUBSTITUTE; METHOD; DATA; TRANSMISSION; SYSTEM; **SYNCHRONOUS** ; **ASYNCHRONOUS** ; DATA; NETWORK; CORRECT; ERROR; TRANSFER; DATA; SUBTRACT; COMPUTATION; CORRECT; VALUE; NUMERIC; VALUE; TRANSMIT; DATA
Derwent Class: W01
International Patent Class (Main): H04L-029/02
International Patent Class (Additional): H04J-003/06; H04L-001/00; H04L-007/00
File Segment: EPI

**19/5/27**
DIALOG(R)File 350:Derwent WPIX


009996914 **Image available**
WPI Acc No: 1994-264625/199433
XRPX Acc No: N94-208222
**Universal protocol** programmable **communications** interface **- has per channel DMA input/output in conjunction with bit level control to support variety of bit oriented communication protocols**
Patent Assignee: EVAN S (EVAN-I); ABB POWER T & D CO INC (ALLM )
Inventor: EVAN S
Number of Countries: 002 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| CA 2112001 | A | 19940622 | CA 2112001 | A | 19931221 | 199433 | B |
| US 5371736 | A | 19941206 | US 92993702 | A | 19921221 | 199503 | |
| CA 2112001 | C | 20000509 | CA 2112001 | A | 19931221 | 200037 | |

Priority Applications (No Type Date): US 92993702 A 19921221
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| CA 2112001 | A | | 39 | G06F-013/42 | |
| US 5371736 | A | | 13 | H04J-003/14 | |
| CA 2112001 | C | E | | G06F-013/42 | |

Abstract (Basic): CA 2112001 A

The interface has a host interface for selectively providing read and write access to the host processor. A data communications controller has a data buffer, a data memory, a DMA device, a data bus and a controller for arbitrating among different requests for access to the data bus. A programmable **synchronous / asynchronous** transceiver is connected to the data bus so as to provide data communications

between the data and a number of data communications devices over the channels. Each transceiver has a programmable word bit length which is programmed independently for each channel to provide serial data communications in the word bit length of the connected device.

ADVANTAGE - Is easily reconfigured or reprogrammed to handle devices with different bit oriented communication protocols.

Dwg.1/4

Title Terms: UNIVERSAL; PROTOCOL; PROGRAM; COMMUNICATE; INTERFACE; PER; CHANNEL; DMA; INPUT; OUTPUT; CONJUNCTION; BIT; LEVEL; CONTROL; SUPPORT; VARIETY; BIT; ORIENT; COMMUNICATE
Index Terms/Additional Words: UART; SART
Derwent Class: T01; W01
International Patent Class (Main): G06F-013/42; H04J-003/14
File Segment: EPI

**19/5/28**

DIALOG(R)File 350:Derwent WPIX


009674684 **Image available**
WPI Acc No: 1993-368237/199346
XRPX Acc No: N93-284305

Asynchronous **replication of data changes by distributed update requests - having computer receiving update and time of transmission and replicating all changes in its database, with computer then updating its control table with time of update transmission**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: EVERSON R S; FELIX M R; ROBERTSON B D
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5261094 | A | 19931109 | US 91682041 | A | 19910408 | 199346 | B |

Priority Applications (No Type Date): US 91682041 A 19910408
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5261094 | A | | 9 | G06F-015/40 | |

Abstract (Basic): US 5261094 A

A first program (TP1) in the Collector node instructs a second program (TP2) in the Collectee node to send all updates to a database since the last conversation. The second program processes queries to retrieve any changes made since the last conversation between the Collector and Collectee nodes and send the data to the first program, which updates the copy of the database on its own system.

The computers communicate in a peer to peer relationship, and are arranged in a hierarchical relationship. Initiation is performed at predefined time **intervals** . The control **table** of each computer includes the time of the last update to the relational database contained in the computer.

ADVANTAGE - Method enables **synchronisation** of changes to relational databases in network.

Dwg.2/6

Title Terms: **ASYNCHRONOUS** ; REPLICA; DATA; CHANGE; DISTRIBUTE; UPDATE; REQUEST; COMPUTER; RECEIVE; UPDATE; TIME; TRANSMISSION; REPLICA; CHANGE; DATABASE; COMPUTER; UPDATE; CONTROL; TABLE; TIME; UPDATE; TRANSMISSION
Derwent Class: T01
International Patent Class (Main): G06F-015/40
International Patent Class (Additional): G06F-015/16
File Segment: EPI

**19/5/29**

DIALOG(R)File 350:Derwent WPIX


003079875

WPI Acc No: 1981-H9915D/198135

**Interface for storing data through video recorder - is under microprocessor control for transfer of data packets to and from recording system**

Patent Assignee: THILO I (THIL-I)
Inventor: THILO I
Number of Countries: 001 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| DE 3005296 | A | 19810820 | | | | 198135 | B |
| DE 3005296 | C | 19820616 | | | | 198225 | |

Priority Applications (No Type Date): DE 3005296 A 19800213
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| DE 3005296 | A | | 9 | | |

Abstract (Basic): DE 3005296 A

A video recorder system provides high data transmission rates. The system is intended for use with personal computers. Data for storage on the video recorder system are transmitted over the data bus (DB) and via a read/write memory (RAM) and is controlled by microprocessor controller (MPU) operating to a programme held in a read only memory (ROM).

**Synchronisation** with line and frame signals is provided by a **programmable interface** unit (PIA). Data blocks are transmitted over an **asynchronous** interface adapter (ACIA) to and from the recorder.

1

Title Terms: INTERFACE; STORAGE; DATA; THROUGH; VIDEO; RECORD; MICROPROCESSOR; CONTROL; TRANSFER; DATA; PACKET; RECORD; SYSTEM
Derwent Class: T03; W04
International Patent Class (Additional): G11B-005/09
File Segment: EPI

```
Set     Items   Description
S1      18328   API OR APPLICATION()PROGRAM?()INTERFACE? OR (APPLICATION? -
             OR PROGRAM?)(2W)INTERFACE?
S2      12784   (TIME()DEPENDENT? OR SYNCHRON?) AND (ASYNCHRON? OR (NON OR
             "NOT")()SYNCHRONOUS)
S3     366581   TIMER? OR TIMING OR TIMESTAMP? OR INTERVAL? OR CLOCK?
S4     992652   END? ? OR TIMEOUT? OR TIME()OUT? ? OR EXPIR?
S5       4851   S3(3N)(DATABASE? OR DATA()(BASE? OR BANK? OR FILE?) OR DAT-
             ABANK? OR DATAFILE? OR TABLE?)
S6     147478   STATEMACHINE? OR STATE()MACHINE? OR CONTROLLER?
S7       4186   INITILIALI? OR REINITIALI?
S8      60400   S3(3N)(MANAG? OR CONTROL? OR ADMINIST? OR MONITOR? OR TRAC-
             K?)
S9         22   S5(S)S2(S)S1
S10        75   S1(S)S2(S)S3
S11        22   S1(S)S2(S)S5
S12        27   S10(S)(S6 OR S7)
S13        28   (S9 OR S11 OR S12) AND IC=G06F?
S14        28   IDPAT (sorted in duplicate/non-duplicate order)
S15        28   IDPAT (primary/non-duplicate records only)
File 348:EUROPEAN PATENTS 1978-2003/Mar W05
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030403,UT=20030327
         (c) 2003 WIPO/Univentio
```

**15/5/1 (Item 1 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS


00711606
**Start code detector for image sequences**
**Detektor fur den Startcode von Bildsequenzen**
**Detecteur de code de depart pour sequences d'images**
PATENT ASSIGNEE:
DISCOVISION ASSOCIATES, (260273), 2355 Main Street Suite 200, Irvine, CA 92714, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucester. GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 674443 A2 950927 (Basic)
EP 674443 A3 951213
EP 674443 A3 981223
EP 674443 B1 010509
APPLICATION (CC, No, Date): EP 95301301 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED DIVISIONAL NUMBER(S) - PN (AN):
EP 891089 (EP 98202149)
(EP 98202154)
EP 884910 (EP 98202132)
EP 891088 (EP 98202133)
EP 897244 (EP 98202134)
EP 901286 (EP 98202135)
EP 901287 (EP 98202166)
EP 896473 (EP 98202170)
EP 896474 (EP 98202171)
EP 896476 (EP 98202174)
EP 896475 (EP 98202172)
INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-013/00 ; G06F-009/38**
CITED PATENTS (EP B): EP 288219 A; EP 460751 A; EP 506294 A; EP 551672 A; EP 572263 A; EP 572766 A; EP 576749 A; EP 577329 A; EP 602621 A; WO 94/25935 A; GB 2269070 A; US 4622585 A; US 4823201 A; US 5173695 A; US 5253053 A
CITED REFERENCES (EP B):
KUN-MIN YANG ET AL: "VLSI ARCHITECTURE DESIGN OF A VERSATILE VARIABLE LENGTH DECODING CHIP FOR REAL-TIME VIDEO CODECS" PROCEEDINGS OF THE REGION 10 CONFERENCE ON COMPUTER AND COMMUNICATI SYSTEMS (TENCON), HONG KONG, 24 - 27 SEPT., 1990, vol. 2, 24 September 1990, pages 551-554, XP000235934 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
KOMORI S ET AL: "AN ELASTIC PIPELINE MECHANISM BY SELF-TIMED CIRCUITS" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 23, no. 1, February 1988, pages 111-117, XP000051576
KAORU UCHIDA ET AL: "A PIPELINED DATAFLOW DATAFLOW PROCESSOR ARCHITECTURE BASED ON A VARIABLE LENGTH TOKEN CONCEPT" ARCHITECTURE, UNIVERSITY PARK, AUG. 15 - 19, 1988, vol. 1, 15 August 1988, pages 209-216, XP000079309 BRIGGS F A
TOKUMICHI MURAKAMI ET AL: "A DSP ARCHITECTURAL DESIGN FOR LOW BIT-RATE MOTION VIDEO CODEC" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, vol. 36, no. 10, 1 October 1989, pages 1267-1274, XP000085313
ELLIOTT J A ET AL: "REAL-TIME SIMULATION OF VIDEOPHONE IMAGE CODING ALGORITHMS ON RECONFIGURABLE MULTICOMPUTERS" IEE PROCEEDINGS E. COMPUTERS & DIGITAL TECHNIQUES, vol. 139, no. 3 PART E, 1 May 1992,

Total word count - documents A + B 255935

**15/5/2 (Item 2 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00967468 **Image available**
**ADAPTIVE CONTROL OF DATA PACKET SIZE IN NETWORKS**
**COMMANDE ADAPTATIVE DES DIMENSIONS DE PAQUETS DE DONNEES DANS DES RESEAUX**
Patent Applicant/Assignee:
INTERNETCLASS COMMUNICATIONS INC, 814 Elm Street, Suites 505-509, Manchester, NH 03101-2130, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
BAHADIROGLU Murat I, 49 Technology Drive, Unit 68, Bedford, NH 03110, US, US (Residence), -- (Nationality), (Designated only for: US)
Legal Representative:
CLAPP Gary D (et al) (agent), Davis & Bujold, P.L.L.C., Fourth Floor, 500 North Commercial Street, Manchester, NH 03101, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 2002101513 A2 20021219 (WO 02101513)
Application: WO 2002US18864 20020611 (PCT/WO US0218864)
Priority Application: US 2001879761 20010612
Parent Application/Grant:
Related by Continuation to: US Not furnished (CIP)
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 28922

English Abstract
An adaptive packet mechanism and method for optimizing data packet transmission through a network connection between a sending node and a receiving node. Current network conditions in the connection are periodically determined wherein the network condition pertain to the latency and jitter of packet transmission between the sending node and receiving node. The measurements of latency and jitter are used to determine an optimum packet size and an optimum inter-packet interval for transmission of packet data between the sending node and the receiving node and are used in the transmission of data packets from the sending node to the receiving node. Network conditions may be determined by transmission of monitor or data packets and may be determined at either or both of the sending or receiving nodes and the optimum packet size and inter-packet interval are determined by a fuzzy logic analyzer, a neural network analyzer or a combined fuzzy/neural network analyzer.

French Abstract
L'invention concerne un mecanisme adaptatif de paquets et un procede permettant d'optimiser une transmission de paquets de donnees dans une connexion de reseau entre un noeud d'emission et un noeud de reception. Des etats reels de reseau dans la connexion sont determines de maniere periodique, l'etat du reseau etant relatif au temps d'attente et a la gigue d'une transmission de paquets entre le noeud d'emission et le noeud de reception. Les mesures du temps d'attente et de la gigue sont utilisees pour determiner des dimensions de paquets optimales et un intervalle entre paquets optimal, aux fins de transmission de paquets de

donnees entre le noeud d'emission et le noeud de reception et sont utilisees pour la transmission de paquets de donnees a partir du noeud d'emission vers le noeud de reception. Des etats de reseau peuvent etre determines par la transmission de paquets de surveillance ou de donnees et peuvent etre determines soit au niveau d'un des deux noeuds, soit au niveau des deux noeuds et les dimensions de paquets optimales et l'intervalle entre paquets optimal sont determines par un analyseur de logique floue, un analyseur de reseau neural ou un analyseur de reseau flou/neural.

Legal Status (Type, Date, Text)
Publication 20021219 A2 Without international search report and to be republished upon receipt of that report.

**15/5/3 (Item 3 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00899480 **Image available**
**MULTIMEDIA SENSOR NETWORK**
**RESEAU DE CAPTEURS MULTIMEDIA**
Patent Applicant/Assignee:
PHYSICAL OPTICS CORPORATION, 20600 Gramercy Place, Torrance, CA 90501, US , US (Residence), US (Nationality)
Inventor(s):
KOSTRZEWSKI Andrew A, 9816 Grouse Court, Garden Grove, CA 92641, US,
RO Sookwang, 315 South Lafayette Park Place #406, Los Angeles, CA 90057, US,
JANNSON Tomasz P, 4629 Via El Sereno, Torrance, CA 90505, US,
CHEN Chih-Jung Judy, 5207 Maricopa Street, Torrance, CA 90503, US,
Legal Representative:
NILLES James E (et al) (agent), Nilles & Nilles, S.C., Firstar Center, Suite 2000, 777 East Wisconsin Avenue, Milwaukee, WI 53202, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200233558 A1 20020425 (WO 0233558)
Application: WO 2001US31799 20011011 (PCT/WO US0131799)
Priority Application: US 2000690149 20001016
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-013/38**
International Patent Class: G08B-013/00; H04N-007/18
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 45207

English Abstract
A multimedia network (10) includes a sensor network (12), a communication bridge (30) and a user network (e.g., the Internet). The sensor network includes a set of interconnected sensors coupled to a control module (56). The control module receives a set of sensed data from the sensors and generates a homogenized data stream based on the sensed data. The communication bridge is coupled to the sensor network and buffers the homogenized data stream. The user network is coupled to the communication bridge and receives the homogenized data stream from the sensor network. The user network transmits data back to the control module through the communication bridge.

French Abstract

La presente invention concerne un reseau (10) multimedia qui comprend un reseau (12) de capteurs, une passerelle de communication (30) et un reseau d'utilisateurs (par exemple l'Internet). Ce reseau de capteurs comprend un ensemble de capteurs interconnectes relie a un module (56) de commande. Ce module de commande recoit un ensemble de donnees captees de ces capteurs et genere un flux de donnees homogeneisees a partir de ces donnees captees. La passerelle de communication est reliee au reseau de capteurs et sert de circuit tampon au flux de donnees homogeneisees. Le reseau d'utilisateurs est relie a la passerelle de communication et recoit ce flux de donnees homogeneisees du reseau de capteurs. Le reseau d'utilisateurs retransmet les donnees au module de commande via la passerelle de communication.

Legal Status (Type, Date, Text)
Publication 20020425 A1 With international search report.
Publication 20020425 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
Examination 20030116 Request for preliminary examination prior to end of 19th month from priority date

**15/5/4 (Item 4 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00893337 **Image available**
**AN EFFICIENT TIMER MANAGEMENT SYSTEM**
**UN SYSTEME EFFICACE DE GESTION DE MINUTERIE**
Patent Applicant/Assignee:
INTERNATIONAL BUSINESS MACHINES CORPORATION, New Orchard Road, Armonk, NY 10504, US, US (Residence), US (Nationality)
IBM UNITED KINGDOM LIMITED, P.O. Box 41, North Harbour, Portsmouth, Hampshire PO6 3AU, GB, GB (Residence), GB (Nationality), (Designated only for: MG)
Inventor(s):
DAMON Philipe, 1000 Smith Level Road Apt S8, Carrboro, NC 27510, US,
HEDDES Marco, 4109 Grand Manor Court # 308, Raleigh, NC 27612, US,
Legal Representative:
JENNINGS Michael John (agent), IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester, Hampshire SO21 2JN, GB,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200227468 A2 20020404 (WO 0227468)
Application: WO 2001GB4322 20010927 (PCT/WO GB0104322)
Priority Application: US 2000675545 20000928
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/00**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 6590

English Abstract
A **timer** management system and method for managing **timers** in both a **synchronous** and **asynchronous** system. In one embodiment of the present invention, a **timer** management system comprises an **application program interface** ( **API** ) for providing a set of **synchronous** functions allowing an application to functionally operate on the **timer** . The **timer** management system further comprises a **timer database** for

storing **timer** -related information. Furthermore, the **timer** management system comprises a **timer** services for detecting the expiring of the **timer** . A handle function of the **timer** services allows an **asynchronous** application, i.e., application in a multi-task system, to **synchronously** act on the **timer** . That is, when a **timer** in a **asynchronous** system times-out, the handle function allows the **asynchronous** application to act on the expired **timer** without incurring an illegal time-out message. In another embodiment of the present invention, a **timer** may be **reinitialized** from the same allocated block of memory used to create the **timer** . In another embodiment of the present invention, a time-out message may be sent using the same allocated block of memory used to create the **timer** .

French Abstract
La presente invention concerne un systeme de gestion de minuterie et un procede de gestion de minuterie a la fois dans un systeme synchrone et asynchrone. Dans un mode de realisation de la presente invention, un systeme de gestion de minuterie comporte une interface applicative (API) fournissant un ensemble de fonctions synchrones permettant une application de fonctionner de maniere operationnelle sur la minuterie. Le systeme de gestion de minuterie comporte en outre une base de donnees pour le stockage d'information associee a la minuterie. Par ailleurs, le systeme de gestion de minuterie comporte des services de minuterie permettant la detection de l'arret de la minuterie. Une fonction de gestion des services de la minuterie permet une application asynchrone, c'est a dire, une application dans un systeme a taches multiples, en vue d'agir sur la minuterie de maniere synchrone. Cela veut dire que lorsqu'une minuterie dans un systeme de gestion asynchrone s'arrete, la fonction de gestion permet l'application asynchrone d'agir sur la minuterie en arret sans entrainer un message de depassement de temps illegal. Dans un autre mode de realisation de l'invention, on peut effectuer la reinitialisation d'une minuterie a partir du meme bloc de memoire alloue pour la generation de la minuterie. Dans encore un autre mode de realisation, on peut emettre un message de depassement de temps imparti en utilisant le meme bloc de memoire utilise pour la generation de la minuterie.

Legal Status (Type, Date, Text)
Publication 20020404 A2 Without international search report and to be republished upon receipt of that report.
Publication 20020404 A2 Published entirely in electronic form (except the front page) and available upon request from the International Bureau.

**15/5/5 (Item 5 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00872937 **Image available**
**A CARD SYSTEM**
**SYSTEME A CARTES**
Patent Applicant/Assignee:
ERG R & D PTY LTD, 247 Balcatta Road, BALCATTA, W.A. 6914, AU, AU (Residence), AU (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
ANDERSON Ian Ronald, 32 Tuscan Road, MANCHESTER, Lancashire M20 5GS, GB, GB (Residence), AU (Nationality), (Designated only for: US)
ABBISS Michael Edward, 4 The Anchorage, MAYLANDS, W.A. 6051, AU, AU (Residence), AU (Nationality), (Designated only for: US)
DENISON Glyn Gregory Horne, 4 Clarendon Street, COTTESLOE, W.A. 6011, AU, AU (Residence), AU (Nationality), (Designated only for: US)
Legal Representative:
WEBBER David (et al) (agent), Davies Collison Cave, 1 Little Collins Street, Melbourne, VIC 3000, AU,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200207071 A1 20020124 (WO 0207071)
Application: WO 2001AU847 20010713 (PCT/WO AU0100847)

Priority Application: AU 20008776 20000713
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G06K-009/62
International Patent Class: G06K-019/06; **G06F-017/60**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 45687

English Abstract
A card system including a plurality of component infrastructures, the component infrastructures each having core components of the system, the infrastructures having a hierarchal relationship such that one infrastructure is dependent on components of a lower infrastructure, and the core components being configurable for different card transaction applications.

French Abstract
L'invention concerne un systeme a cartes dote d'une pluralite d'infrastructures de composants, lesquelles comprennent chacune des composants de base de ce systeme. Lesdites infrastructures sont mises en relation hierarchique de facon qu'une infrastructure donnee depende des composants d'une infrastructure inferieure, les composants de base pouvant etre configures pour differentes applications de transactions par cartes.

Legal Status (Type, Date, Text)
Publication 20020124 A1 With international search report.
Rev Srch Rpt 20020321 Late publication of revised international search report
Republication 20020321 A1 With international search report.
Examination 20020418 Request for preliminary examination prior to end of 19th month from priority date

**15/5/6 (Item 6 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00857190 **Image available**
**A NETWORK DEVICE FOR SUPPORTING MULTIPLE UPPER LAYER NETWORK PROTOCOLS OVER A SINGLE NETWORK CONNECTION**
**DISPOSITIF DE RESEAU COMPATIBLE AVEC PLUSIEURS PROTOCOLES DE RESEAU A COUCHE SUPERIEURE VIA UNE SEULE CONNEXION RESEAU**
Patent Applicant/Assignee:
EQUIPE COMMUNICATIONS CORPORATION, 100 Nagog Park, Acton, MA 01720, US, US (Residence), US (Nationality)
Inventor(s):
BLACK Darryl, 14 Hills Farm Lane, Hollis, NH 03049, US,
LANGRIND Nicholas A, 8 Bedford Road, Carlisle, MA 01741, US,
WHITESEL Richard L, 22 Shingle Mill Drive, Nashua, NH 03062, US,
PERRY Thomas R, 230 Hayden Road, Groton, MA 01450, US,
KIDDER Joseph D, 31 Bonad Road, Arlington, MA 02476, US,
SULLIVAN Daniel J, 35 Glen Road, Hopkinton, MA 01748, US,
FOX Barbara A, 67 Eliot Park, Arlington, MA 02474, US,
MADSEN Jonathon D, 34 Park Avenue Extn., Arlington, MA 02474, US,
PROVENCHER Roland T, 28 Richman Road, Hudson, NH 03051, US,
PEARSON Terrence S, 8 Hills Farm Lane, Hollis, NH 03049, US,
BHATT Umesh, 26 Brackenwood Drive, Nashua, NH 03062, US,

POTHIER Peter, 54 Maplewood Drive, Townsend, MA 01469, US,
MANOR Larry B, 15 Cross Road, Londonderry, NH 03053, US,
Legal Representative:
ENGELLENNER Thomas J (et al) (agent), Nutter, McClennen & Fish, LLP, One International Place, Boston, MA 02110-2699, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200190843 A2-A3 20011129 (WO 0190843)
Application: WO 2001US15867 20010516 (PCT/WO US0115867)
Priority Application: US 2000574343 20000520; US 2000574341 20000520; US 2000574440 20000520; US 2000588398 20000606; US 2000591193 20000609; US 2000593034 20000613; US 2000596055 20000616; US 2000613940 20000711; US 2000616477 20000714; US 2000625101 20000724; US 2000633675 20000807; US 2000637800 20000811; US 2000653700 20000831; US 2000656123 20000906; US 2000663947 20000918; US 2000669364 20000926; US 2000687191 20001012; US 2000703856 20001101; US 2000711054 20001109; US 2000718224 20001121; US 2001756936 20010109; US 2001777468 20010205; US 2001789665 20010221; US 2001803783 20010312; US 2001832436 20010410
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-013/00**
International Patent Class: **G06F-017/30** ; **G06F-001/18** ; **G06F-011/30** ; **G06F-012/14** ; **G06F-003/14** ; H04L-012/56; H04M-001/10; H04M-007/00; H04M-003/00; H01J-003/14
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 210510

English Abstract
The present invention provides a network device with at least one physical interface or port (44,68) that is capable of transferring network packets including data organized into one or more upper layer network protocols. Network packets are received by the port (44,68) and a port subsystem in accordance with a physical layer network protocol and transferred to forwarding subsystems within the network device in accordance with the upper layer protocols into which the network packets data has been organized. Network packets including data organized in accordance with ATM are then transferred to one or more ATM forwarding subsystems, network packets including data organized in accordance with MPLS are transferred to one or more MPLS forwarding subsystems, and network packets including data organized in accordance with IP are transferred to one or more IP forwarding subsystems.

French Abstract
L'invention concerne un dispositif de reseau comportant au moins une interface ou port physique pouvant transferer des paquets de reseau contenant des donnees organisees en un ou plusieurs protocoles reseau a couche superieure (par exemple, ATM, MPLS, IP, Frame Relay, Voice, Circuit Emulation). Ledit port peut etre connecte a une annexe de reseau afin de permettre que le dispositif de reseau puisse transferer des paquets de reseau avec d'autres dispositifs de reseau. Des paquets de reseau sont recus par le port et un sous-systeme de port conforme a un protocole de reseau a couche physique, puis transferes vers des sous-systemes de reexpedition a l'interieur du dispositif de reseau conformes aux protocoles a couche superieure dans lesquels les donnees de paquets de reseau ont ete organisees. Par exemple, les donnees organisees conformement a ATM via SONET, MPLS via SONET et IP via SONET peuvent etre transferees via une annexe de reseau vers un port du dispositif de reseau. Les paquets de reseau contenant des donnees organisees conformement a ATM sont ensuite transferes vers un ou plusieurs

sous-systemes de reexpedition ATM et les paquets de reseau contenant des donnees organisees conformement a IP sont transferes sur un ou plusieurs sous-systemes de reexpedition IP. Pour une efficacite accrue, ce dispositif de reseau permet a l'administrateur de reseau de n'ajouter que le nombre et les types de sous-systemes de reexpedition necessaires pour repondre au service de reseau souscrit pour chaque protocole de reseau a couche. Par ailleurs, ce dispositif de reseau peut necessiter moins d'interfaces physiques que les dispositifs de reseau anterieurs.

Legal Status (Type, Date, Text)
Publication 20011129 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20020704 Late publication of international search report
Republication 20020704 A3 With international search report.
Examination 20021205 Request for preliminary examination prior to end of 19th month from priority date

**15/5/7 (Item 7 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00806383
**COLLABORATIVE CAPACITY PLANNING AND REVERSE INVENTORY MANAGEMENT DURING DEMAND AND SUPPLY PLANNING IN A NETWORK-BASED SUPPLY CHAIN ENVIRONMENT AND METHOD THEREOF**
**PLANIFICATION EN COLLABORATION DES CAPACITES ET GESTION ANTICIPEE DES STOCKS LORS DE LA PLANIFICATION DE L'OFFRE ET DE LA DEMANDE DANS UN ENVIRONNEMENT DE CHAINE D'APPROVISIONNEMENT FONDEE SUR LE RESEAU ET PROCEDE ASSOCIE**
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
MIKURAK Michael G, 108 Englewood Blvd., Hamilton, NJ 08610, US,
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly, LLP, 1400 Page Mill Road, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200139029 A2 20010531 (WO 0139029)
Application: WO 2000US32309 20001122 (PCT/WO US0032309)
Priority Application: US 99444655 19991122; US 99444886 19991122
Designated States: AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/60**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 157840

English Abstract

French Abstract

Legal Status (Type, Date, Text)
Publication 20010531 A2 Without international search report and to be republished upon receipt of that report.
Examination 20011206 Request for preliminary examination prior to end of

19th month from priority date
Declaration 20030103 Late publication under Article 17.2a
Republication 20030103 A2 With declaration under Article 17(2)(a); without abstract; title not checked by the International Searching Authority.

**15/5/8 (Item 8 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00784185 **Image available**
**A SYSTEM AND METHOD FOR STREAM-BASED COMMUNICATION IN A COMMUNICATION SERVICES PATTERNS ENVIRONMENT**
**SYSTEME, PROCEDE ET ARTICLE DE PRODUCTION FOURNISSANT UN SYSTEME DE COMMUNICATION EN CONTINU DANS UN ENVIRONNEMENT DE CONFIGURATIONS DE SERVICES DE COMMUNICATION**
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
HICKMAN Paul L (agent), Hickman Coleman & Hughes, LLP, P.O. Box 52037, Palo Alto, CA 94303-0746, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200117195 A2-A3 20010308 (WO 0117195)
Application: WO 2000US24125 20000831 (PCT/WO US0024125)
Priority Application: US 99386717 19990831
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H04L-029/06
International Patent Class: **G06F-017/22** ; H04L-029/12
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150532

English Abstract
A system, method, and article of manufacture are disclosed for providing a stream-based communication system. A shared format is defined on interface code for a sending system and a receiving system. A message to be sent from the sending system to the receiving system is translated based on the shared format. Once translated, the message is then sent from the sending system and received by the receiving system. Once the message is received by the receiving system, the message is then translated based on the shared format.

French Abstract
L'invention concerne un systeme, un procede et un article de production fournissant un systeme de communication en continu. Un format partage est defini selon un code d'interface pour un systeme emetteur et un systeme recepteur. Un message devant etre envoye par le systeme emetteur est traduit sur la base du format partage. Une fois traduit, le message est envoye du systeme emetteur et recu par le systeme recepteur. Le message recu par le systeme recepteur est ensuite traduit sur la base du format partage.

Legal Status (Type, Date, Text)

Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010907 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20011115 Late publication of international search report
Republication 20011115 A3 With international search report.

**15/5/9 (Item 9 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00784140
**A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A GLOBALLY ADDRESSABLE INTERFACE IN A COMMUNICATION SERVICES PATTERNS ENVIRONMENT**
**SYSTEME, PROCEDE ET ARTICLE DE FABRICATION S'APPLIQUANT DANS UN ENVIRONNEMENT DE STRUCTURE DE SERVICES DE COMMUNICATIONS VIA UNE INTERFACE ADRESSABLE GLOBALEMENT**
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly, LLP, 1400 Page Mill Road, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116735 A2-A3 20010308 (WO 0116735)
Application: WO 2000US24198 20000831 (PCT/WO US0024198)
Priority Application: US 99387214 19990831
Designated States: AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CU CZ DE DK DZ EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/46**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150371

English Abstract
A system, method, and article of manufacture are provided for delivering service via a globally addressable interface. A plurality of interfaces are provided with access allowed to a plurality of different sets of services from each of the interfaces. Each interface has a unique set of services associated therewith. Each of the interfaces is named with a name indicative of the unique set of services associated therewith. The names of the interfaces are then broadcast to a plurality of systems requiring service.

French Abstract
L'invention porte sur un systeme, un procede et un article de fabrication appliques dans la distribution de services via une interface adressable globalement. Une pluralite d'interfaces permettent d'acceder a une pluralite de differents ensembles de services. A chaque interface est associe un ensemble unique de services. Chacune de ces interfaces est affectee d'un nom designant l'ensemble unique de services correspondant. Les noms des interfaces sont ensuite diffuses a une pluralite de systemes requerant un service.

Legal Status (Type, Date, Text)

Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010927 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20030109 Late publication of international search report
Republication 20030109 A3 With international search report.

**15/5/10 (Item 10 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00784139
**A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A SELF-DESCRIBING STREAM IN A COMMUNICATION SERVICES PATTERNS ENVIRONMENT**
**SYSTEME, PROCEDE ET ARTICLE DE FABRICATION DESTINES A UN FLUX D'AUTODESCRIPTEURS DANS UN ENVIRONNEMENT DE MODELES DE SERVICES DE COMMUNICATION**
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly, LLP, 1400 Page Mill Road, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116734 A2-A3 20010308 (WO 0116734)
Application: WO 2000US23999 20000831 (PCT/WO US0023999)
Priority Application: US 99387070 19990831
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/46**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150517

English Abstract
A system, method, and article of manufacture are described for providing a self-describing stream-based communication system. Messages are sent which include data between a sending system and a receiving system. Meta-data is attached to the messages being sent between the sending system and the receiving system. The data of the messages sent from the sending system to the receiving system is translated based on the meta-data. The meta-data includes first and second sections. The first section identifies a type of object associated with the data and a number of attribute descriptors in the data. The second section includes a series of the attribute descriptors defining elements of the data.

French Abstract
L'invention concerne un systeme, un procede et un article de fabrication destines a constituer un systeme de communication a base d'un flux d'autodescripteurs. Des messages comprenant des donnees sont envoyes, entre un systeme expediteur et un systeme recepteur. Des metadonnees sont attachees aux messages en cours d'envoi entre le systeme expediteur et le systeme recepteur. Les donnees des messages envoyes du systeme expediteur au systeme recepteur sont traduites d'apres les metadonnees, lesquelles comprennent des premiere et seconde sections. La premiere section

identifie un type d'objet associe aux donnees et un nombre de descripteurs d'attributs presents dans celles-ci. La seconde section comprend une serie de descripteurs d'attributs definissant des elements des donnees.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010927 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20020221 Late publication of international search report
Republication 20020221 A3 With international search report.

**15/5/11 (Item 11 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00784137
**SYSTEM, METHOD, AND ARTICLE OF MANUFACTURE FOR DISTRIBUTED GARBAGE COLLECTION IN ENVIRONMENT SERVICES PATTERNS**
**SYSTEME, PROCEDE ET ARTICLE DE FABRICATION EN MATIERE DE RECUPERATION D'ESPACE REPARTI DANS DES MOTIFS DE SERVICES D'ENVIRONNEMENT**
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6416 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly, LLP, 1400 Page Mill Road, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116729 A2-A3 20010308 (WO 0116729)
Application: WO 2000US24238 20000831 (PCT/WO US0024238)
Priority Application: US 99386435 19990831
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/44**
International Patent Class: **G06F-009/46**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150959

English Abstract
A system, method and article of manufacture are provided for detecting an orphaned server context. A collection of outstanding server objects is maintained and a list of contexts is created for each of the outstanding server objects. A compilation of clients who are interested in each of the outstanding server objects are added to the list. Recorded on the list is a duration of time since the clients invoked a method accessing each of the contexts of the outstanding server objects. The list is examined at predetermined intervals for determining whether a predetermined amount of time has passed since each of the objects has been accessed. Contexts that have not been accessed in the predetermined amount of time are selected and information is sent to the clients identifying the contexts that have not been accessed in the predetermined amount of time.

French Abstract
L'invention concerne un systeme, un procede et un article de fabrication permettant de detecter un contexte de serveur a l'abandon. On conserve une collection d'objets de serveur en cours et on cree une liste de contextes pour chaque objet dudit serveur, a laquelle on ajoute une compilation de clients s'interessant a chaque objet de serveur en cours. On enregistre sur la liste une duree a partir du moment ou les clients lancent un procede leur permettant d'acceder a chaque contexte des objets de serveur en cours. La liste est examinee a des intervalles predetermines pour etablir si, depuis l'acces auxdits objets, un delai predetermine s'est ecoule ou non. Les contextes auxquels on n'a pas accede dans le delai predetermine sont selectionnes et les clients informes de l'identite de ces contextes.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20021227 Late publication of international search report
Republication 20021227 A3 With international search report.

**15/5/12 (Item 12 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00784134
**A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A CONSTANT CLASS COMPONENT IN A BUSINESS LOGIC SERVICES PATTERNS ENVIRONMENT**
**SYSTEME, PROCEDE ET ARTICLE MANUFACTURE UN COMPOSANT DE CLASSE DE CONSTANTE DANS UN ENVIRONNEMENT DE SCHEMAS DE SERVICES DE LOGIQUE D'AFFAIRES**
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly LLP, Suite 3800, 2029 Century Park East, Los Angeles, CA 90067-3024, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116726 A2-A3 20010308 (WO 0116726)
Application: WO 2000US24188 20000831 (PCT/WO US0024188)
Priority Application: US 99387213 19990831
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/44**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150446

English Abstract
A system, method, and article of manufacture are provided for managing constants in a computer program. A plurality of constant names are provided. Each of the constant names has a corresponding constant value. The constant names are grouped into constant classes based on an entity which the constant values represents. Access is allowed to the constant values by receiving a call including the corresponding constant name and corresponding constant class.
French Abstract

L'invention porte sur un systeme, un procede et un article de gestion des constantes d'un programme d'ordinateur. On etablit les noms de differentes constantes a chacun desquels correspond la valeur d'une constante, puis les noms sont regroupes par classes de constantes en fonction d'une entite representant les valeurs des constantes. L'acces a une valeur de constante est autorise lors de la reception d'un appel comprenant le nom et la classe de la constante correspondante.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010809 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20020502 Late publication of international search report
Republication 20020502 A3 With international search report.

**15/5/13 (Item 13 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00784132
**A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A LEGACY WRAPPER IN A COMMUNICATION SERVICES PATTERNS ENVIRONMENT**
**SYSTEME, PROCEDE ET DISPOSITIF POUR MODULE D'HABILLAGE EXISTANT DANS UN ENVIRONNEMENT DE SCHEMAS DE SERVICES DE COMMUNICATION**
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918 , US,
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly, LLP, 1400 Page Mill Roadast, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116724 A2-A3 20010308 (WO 0116724)
Application: WO 2000US24084 20000831 (PCT/WO US0024084)
Priority Application: US 99386834 19990831
Designated States: AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CU CZ DE DK DZ EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/44**
International Patent Class: **G06F-009/46**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150947

English Abstract
A system, method, and article of manufacture are provided for affording access to a legacy system. A plurality of components coupled to a client via a component integration architecture are provided for servicing the client. A legacy system is interconnected to the client via the integration architecture using a legacy wrapper. The legacy system and the client are interfaced via the legacy wrapper by communicating with the client by way of a first protocol and by communicating with the legacy system by way of a second protocol.

French Abstract
Cette invention concerne un systeme, un procede et un dispositif donnant

acces a un systeme existant. Une pluralite de composants relies a un client via une architecture d'integration de composants est mise a la disposition du client. Un systeme existant est interconnecte via l'architecture d'integration au moyen d'un module d'habillage existant. Le systeme existant et le client sont mis en interface via le module d'habillage existant, la communication avec le client se faisant au moyen d'un premier protocole, celle avec le systeme existant au moyen d'un second protocole.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20011011 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20020620 Late publication of international search report
Republication 20020620 A3 With international search report.

**15/5/14 (Item 14 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00784125
**SYSTEM, METHOD, AND ARTICLE OF MANUFACTURE FOR PIECEMEAL RETRIEVAL IN AN INFORMATION SERVICES PATTERNS ENVIRONMENT**
**SYSTEME, PROCEDE ET ARTICLE DE FABRICATION DESTINES A LA RECHERCHE FRAGMENTAIRE DANS UN ENVIRONNEMENT DE MODELES DE SERVICES D'INFORMATIONS**
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly, LLP, 38th Floor, 2029 Century Park East, Los Angeles, CA 90067-3024, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116705 A2-A3 20010308 (WO 0116705)
Application: WO 2000US24085 20000831 (PCT/WO US0024085)
Priority Application: US 99386433 19990831
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/44**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150355

English Abstract
A system, method and article of manufacture are provided for providing a warning upon retrieval of objects that are incomplete. An object is provided with at least one missing attribute. Upon receipt of a request from an application for the object access to the attributes of the object is allowed by the application. A warning is provided upon an attempt to access the attribute of the object that is missing.
French Abstract
L'invention concerne un systeme, un procede et un article de fabrication concus pour emettre un avertissement lors de l'extraction d'objets qui sont incomplets. L'objet fourni presente au moins un attribut manquant.

Des la reception d'une requete d'une application pour l'objet, ladite application autorise l'acces aux attributs de cet objet. Un avertissement est emis lorsque l'on tente d'acceder a l'attribut manquant de l'objet.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20011018 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20011122 Late publication of international search report
Republication 20011122 A3 With international search report.

**15/5/15 (Item 15 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00784124
**SYSTEM, METHOD, AND ARTICLE OF MANUFACTURE FOR A REQUEST SORTER IN A TRANSACTION SERVICES PATTERNS ENVIRONMENT**
**SYSTEME, PROCEDE ET ARTICLE DE FABRICATION APPLIQUES DANS UN TRIEUR DE REQUETES D'UN ENVIRONNEMENT DE STRUCTURES DE SERVICES DE TRANSACTIONS**
Patent Applicant/Assignee:
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Inventor(s):
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Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly, LLP, 38th floor, 2029 Century Park East, Los Angeles, CA 90067-3024, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116704 A2-A3 20010308 (WO 0116704)
Application: WO 2000US24082 20000831 (PCT/WO US0024082)
Priority Application: US 99386715 19990831
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/46**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150733

English Abstract
A system, method and article of manufacture are provided for sorting requests that are being unbatched from a batched message. A group of business objects necessary for a transaction are provided. Logically-related requests received from the business objects are grouped. Sorting rules and/or sort weights are obtained and the requests in the message are sorted and placed in a specific order determined from the sorting rules and/or the sort weights. The sorted requests are batched into a single message which is sent to a data server where the requests are unbundled from the message in the specific order.

French Abstract
L'invention porte sur un systeme, un procede et un article de fabrication utilises dans le tri de requetes qui sont desolidarisees d'un message traite par lots. L'invention porte egalement sur un groupe d'objets commerciaux destines a etre utilises dans une transaction. Les requetes relatives a une logique et provenant d'objets commerciaux sont groupees.

Des regles et/ou des poids de tri sont obtenus et les requetes du message sont triees et placees dans un ordre specifique, determine a partir des regles et/ou des poids de tri. Les requetes triees sont traitees par lots dans un message unique qui est envoye a un serveur de donnees ou les requetes sont desolidarisees du message dans l'ordre specifique.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010809 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20011206 Late publication of international search report
Republication 20011206 A3 With international search report.

**15/5/16 (Item 16 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00777012
**A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR PROVIDING AN INTERFACE BETWEEN A FIRST SERVER AND A SECOND SERVER.**
**SYSTEME, PROCEDE ET ARTICLE MANUFACTURE DESTINES A UNE ARCHITECTURE DE COMMERCE ELECTRONIQUE BASEE SUR JAVA**
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
UNDERWOOD Roy A, 4436 Hearthmoor Court, Long Grove, IL 60047, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly, LLP, 38th floor, 2029 Century Park East, Los Angeles, CA 90067-3024, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200109721 A2-A3 20010208 (WO 0109721)
Application: WO 2000US20561 20000728 (PCT/WO US0020561)
Priority Application: US 99364531 19990730
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/46**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 126924

English Abstract
A system, method and article of manufacture are provided for providing an interface between a first server and a second server with a proxy component situated therebetween. Initially, a request for a business object is identified by an application on the first server. The first server is then connected to the second server. Next, selection criteria from the first server is transmitted to the second server. In response to the selection criteria, the first server receives a first recordset and a second recordset from the second server. Business data is included in the first recordset and result codes are included in the second recordset. The first and second recordsets are mapped to the business object and the business object is sent to the application on the first server.

French Abstract
L'invention concerne un systeme, un procede et un article manufacture

destines a fournir une interface entre un premier et un second serveurs avec, entre les deux, un composant mandataire. A l'origine, une demande d'objet commercial est identifiee par une application sur le premier serveur, lequel est alors relie au second serveur. Puis, des criteres de selection sont transmis du premier au second serveurs. En reponse aux criteres de selection, le premier serveur recoit du second serveur un premier puis un second ensembles d'articles. Des donnees commerciales sont incluses dans le premier ensemble d'articles et des codes de resultats dans le second ensemble d'articles. Une correspondance est etablie entre les premier et second ensembles d'articles et l'objet commercial, lequel est envoye a l'application sur le premier serveur.

Legal Status (Type, Date, Text)
Publication 20010208 A2 Without international search report and to be republished upon receipt of that report.
Examination 20020321 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20020510 Late publication of international search report
Republication 20020510 A3 With international search report.

**15/5/17 (Item 17 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00761431
**A SYSTEM, METHOD, AND ARTICLE OF MANUFACTURE FOR PROVIDING COMMERCE-RELATED WEB APPLICATION SERVICES**
**SYSTEME, PROCEDE ET ARTICLE MANUFACTURE DESTINES A LA FOURNITURE DE SERVICES D'APPLICATION DANS LE WEB LIES AU COMMERCE**
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Legal Representative:
BRUESS Steven C (agent), Merchant & Gould P.C., P.O. Box 2903, Minneapolis, MN 55402-0903, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200073957 A2-A3 20001207 (WO 0073957)
Application: WO 2000US14420 20000525 (PCT/WO US0014420)
Priority Application: US 99321492 19990527
Designated States: AE AG AL AM AT AT (utility model) AU AZ BA BB BG BR BY CA CH CN CR CU CZ CZ (utility model) DE DE (utility model) DK DK (utility model) DM DZ EE EE (utility model) ES FI FI (utility model) GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KR (utility model) KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SK (utility model) SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/30**
International Patent Class: **G06F-017/60 ; G06F-009/44**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150171

English Abstract
A system, method, and article of manufacture are provided that afford a combination of commerce-related web application services. Various features are included such as allowing purchase of products and services via a displayed catalog. As an option, such catalog may be personalized.

In various embodiments, a virtual shopping cart environment may be provided. Further, data, i.e. specifications, details, etc., relating to the products and services may be displayed along with a comparison between different products and services. Data relating to needs of a user may also be received for the purpose of outputting a recommendation of the products and services based on the inputted needs. Optionally, features of the products and services may be listed in order to allow the user to configure a specifically tailored product or service. Yet another aspect of the present invention includes outputting an estimate relating to a price and/or availability of the products and services. Further, an order for the products and services may be received after which a tax and a shipping fee are calculated. A status of the delivery of the ordered products and services may also be provided.

French Abstract
L'invention concerne un systeme, un procede et un article manufacture destines a la fourniture d'une combinaison de services d'application dans le Web lies au commerce. Le systeme presente plusieurs caracteristiques telles que l'achat de produits et de services grace a un catalogue affiche. En option, ce catalogue peut etre personnalise. Plusieurs modes de realisation peuvent comprendre un environnement de chariot de supermarche virtuel. En outre, des donnees, c.-a-d. des specifications, des details, etc., se rapportant aux produits et services peuvent etre affichees en meme temps qu'une comparaison entre differents produits et services. On peut aussi inclure des donnees relatives aux besoins d'un utilisateur afin de recommander des produits et services donnes sur la base des besoins entres. Eventuellement, on peut etablir une liste des caracteristiques des produits et services afin de permettre a l'utilisateur de configurer un produit ou un service personnalise. Dans un autre aspect de la presente invention, on peut produire une estimation du prix et/ou de la disponibilite des produits et services. En outre, une commande peut etre recue et une taxe et des frais d'expedition calcules. Un etat de l'expedition des produits et services commandes peut egalement etre etabli.

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Examination 20010222 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20010816 Late publication of international search report
Republication 20010816 A3 With international search report.

**15/5/18 (Item 18 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00753758 **Image available**
**DATA TRANSFER, SYNCHRONISING APPLICATIONS, AND LOW LATENCY NETWORKS**
**TRANSFERT DE DONNEES, SYNCHRONISATION D'APPLICATIONS ET RESEAU A FAIBLE TEMPS D'ATTENTE**

Patent Applicant/Assignee:
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MAPP Glenford Ezra, 30 Mowbray Road, Cambridge CB1 7SY, GB, GB (Residence), GB (Nationality), (Designated only for: US)
HODGES Stephen John, 12 Petersham Mews, Kensington, London SW7 5NR, GB, GB (Residence), GB (Nationality), (Designated only for: US)
Legal Representative:
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Patent and Priority Information (Country, Number, Date):
  Patent: WO 200067131 A2-A3 20001109 (WO 0067131)
  Application: WO 2000GB1691 20000503 (PCT/WO GB0001691)
  Priority Application: GB 9910280 19990504
Designated States: US
  (EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-009/46**
International Patent Class: H04L-029/06
Publication Language: English
Filing Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 23860

English Abstract
  A synchronous network interface and method of synchronisation between two applications on different computers is provided. The network interface contains snooping hardware which can be programmed to contain triggering values comprising either addresses, address ranges or other data which are to be matched. These data are termed "trip wires". Once programmed, the interface monitors the data stream, including address data, passing through the interface for addresses and data which match the trip wires which have been set. On a match, the snooping hardware can generate interrupts, increment event counters, or perform some other application-specified action. This snooping hardware is preferably based upon Content-Addressable Memory. The invention thus provides in-band synchronisation by using synchronisation primitives which are programmable by user level applications, while still delivering high bandwidth and low latency. The programming of the synchronisation primitives can be made by the sending and receiving applications independently of each other and no synchronisation information is required to traverse the network.

French Abstract
  Cette invention concerne une interface de reseau asynchrone ainsi qu'un procede de synchronisation entre deux applications tournant sur des ordinateurs distincts. Cette interface de reseau comprend un materiel de surveillance qui peut etre programme de maniere a contenir des valeurs de declenchement comprenant soit des adresses, des eventails d'adresses ou d'autres donnees devant etre mises en correspondance. Ces donnees sont appelees fils-pieges (trip wires). Une fois programmee, l'interface controle le flux de donnees, y compris les donnees d'adresse, qui passent par elle afin de deceler des adresses et des donnees qui correspondent aux fils-pieges etablis. En cas de correspondance, le materiel de surveillance peut lancer des interruptions, incrementer des compteurs d'evenements ou effectuer une autre action specifiee par l'application. Ce materiel de surveillance est de preference du type memoire a contenu adressable. Cette invention permet ainsi d'obtenir une synchronisation intrabande en utilisant des primitives de synchronisation qui sont programmables par des applications de niveau utilisateur, ceci tout en offrant une largeur de bande elevee et un faible temps d'attente. La programmation des primitives de synchronisation peut se faire en envoyant et en recevant des applications independamment les unes des autres, aucune information de synchronisation ne devant traverser le reseau.

Legal Status (Type, Date, Text)
Publication 20001109 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010104 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20010913 Late publication of international search report
Republication 20010913 A3 With international search report.

**15/5/19 (Item 19 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT

00505506 **Image available**

**DATA TRANSFERRING IN SOURCE-SYNCHRONOUS AND COMMON CLOCK PROTOCOLS**

**TRANSFERT DE DONNEES SELON' DES PROTOCOLES DE TRANSMISSION DE SOURCE SYNCHRONE ET A HORLOGE COMMUNE**

Patent Applicant/Assignee:
INTEL CORPORATION,
MACWILLIAMS Peter D,
WU William S,
SAMPATH Dilip K,
PRASAD Bindi A,

Inventor(s):
MACWILLIAMS Peter D,
WU William S,
SAMPATH Dilip K,
PRASAD Bindi A,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9936858 A1 19990722
Application: WO 99US199 19990105 (PCT/WO US9900199)
Priority Application: US 986322 19980113

Designated States: AL AM AT AT AU AZ BA BB BG BR BY CA CH CN CU CZ CZ DE DE DK DK EE EE ES FI FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

Main International Patent Class: **G06F-013/42**

Publication Language: English

Fulltext Availability:
Detailed Description
Claims

Fulltext Word Count: 6448

English Abstract

A method and apparatus for transferring data between bus agents (102-105) in a computer system (100). The present invention includes transmitting a control signal (428, 426), from a first agent (102-105) to a second agent (102-105), via a first transfer protocol; and transmitting data (308) corresponding to the control signal (428, 426), from the first agent (102-105) to the second agent (102-105), via a second transfer protocol. In one embodiment, the control signals (428, 426) are transmitted from the first agent (102-105) to the second agent (102-105) via a synchronous transmission with respect to a bus clock (600); and, the data is transmitted via an asynchronous transmission with respect to the bus clock (600). The synchronous transmission is a common clock data transfer protocol, and the asynchronous transmission is a source clock data transfer protocol.

French Abstract

L'invention concerne un procede et un appareil servant a transferer des donnees entre des agents (102-105) de bus dans un systeme (100) d'ordinateurs. Le procede comprend les etapes consistant a transmettre un signal (428, 426) de commande, d'un premier agent (102-105) a un deuxieme agent (102-105) au moyen d'un premier protocole de transfert; et transmettre des donnees (308) correspondant au signal (428, 426) de commande, du premier agent (102-105) a un deuxieme agent (102-105) au moyen d'un deuxieme protocole de transfert. Dans un mode de realisation, les signaux (428, 426) de commande sont transmis du premier agent (102-105) au deuxieme agent (102-105) au moyen d'une transmission synchrone par rapport a une horloge (600) de bus; et les donnees sont transmises au moyen d'une transmission asynchrone par rapport a l'horloge (600) de bus. La transmission synchrone est un protocole de transfert de donnees a horloge commune, et la transmission asynchrone est un protocole de transfert de donnees d'horloge source.

**15/5/20 (Item 20 from file: 349)**

DIALOG(R)File 349:PCT FULLTEXT

00487161 **Image available**

**MODEM CONTROL**

**COMMANDE DE MODEM**

Patent Applicant/Assignee:
CANAL+ SOCIETE ANONYME,
MERIC Jerome,
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Inventor(s):
MERIC Jerome,
BEUQUE Jean-Bernard Gerard Maurice,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9918513 A1 19990415
Application: WO 98IB1606 19981002 (PCT/WO IB9801606)
Priority Application: EP 97402334 19971003

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

Main International Patent Class: **G06F-013/38**

International Patent Class: **G06F-013/10**

Publication Language: English

Fulltext Availability:
Detailed Description
Claims

Fulltext Word Count: 6808

English Abstract

A modem device driver, particularly for use in a receiver/decoder (2020) for a digital broadcast system in which received signals are passed through a receiver to the receiver/decoder and thence to a television set. The receiver/decoder is controlled by a virtual machine (4007) which includes a run time engine (4008). The receiver/decoder includes a plurality of interfaces to external units, and logical driver devices for the interfaces. A device driver (500) for controlling a modem interface comprises a buffer memory (503) for receiving messages, a control memory (502) for storing control parameters, and a logic unit (501) for controlling the device driver and the flow of messages. The logic unit includes a comparator (511) for matching Event, ACK, and NACK patterns stored in the control memory against the end of messages stored in the buffer memory.

French Abstract

L'invention concerne un pilote de modem, a utiliser specifiquement dans un recepteur/decodeur (2020) pour un systeme de radiodiffusion numerique, dans lequel les signaux sont envoyes par un recepteur au recepteur/decodeur puis a un poste de television. Le recepteur/decodeur est commande par une machine virtuelle (400) qui comprend un moteur valorise a l'execution (4008). Le recepteur/decodeur comprend plusieurs interfaces avec des unites externes, et des dispositifs pilotes logiques pour les interfaces. Un pilot d'interface (500) pour commander une interface de modem comprend une memoire tampon (503) qui recoit les messages, une memoire de commande (502) qui memorise les parametres de commande, et une unite logique (501) pour commander le pilote du dispositif et l'acheminement des messages. L'unite logique comporte un comparateur (511) pour mettre en correspondance les modeles d'EVENEMENT, D'ACCUSE RECEPTION POSITIF, D'ACCUSE RECEPTION NEGATIF memorises dans la memoire de commande, avec la fin des messages memorises dans la memoire tampon.

**15/5/21 (Item 21 from file: 349)**

DIALOG(R)File 349:PCT FULLTEXT



00431190 **Image available**

**LOG BASED DATA ARCHITECTURE FOR A TRANSACTIONAL MESSAGE QUEUING SYSTEM**
**ARCHITECTURE DE DONNEES A JOURNALISATION POUR SYSTEME TRANSACTIONNEL DE GESTION DE FILES D'ATTENTE DE MESSAGES**

Patent Applicant/Assignee:
MITSUBISHI ELECTRIC INFORMATION TECHNOLOGY CENTER AMERICA INC,
Inventor(s):
WONG David W H,
SCHWENKE Derek L,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9821654 A1 19980522
Application: WO 97US20561 19971111 (PCT/WO US9720561)
Priority Application: US 9630905 19961114
Designated States: AU CA CN IL JP KR MX NO NZ SG AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-011/00**
International Patent Class: **G06F-12:00**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 104413

English Abstract
A message queuing system is provided that saves and stores messages and their state in an efficient single file on a single disk to enable rapid recovery from server failures. The single disk, single file storage system into which messages and their states are stored eliminates writes to three different disks, the data disk, the index structure disk and the log disk. The single disk, single file storage is made possible by clustering all information together in a contiguous space on the same disk. The result is that all writes are contained in one sweeping motion of the write head in which the write head moves only in one direction and only once to find the area where it needs to start writing messages and their states are stored. In order to keep track of the clustered information, a unique Queue Entry Map Table (100) is used which includes control information (100), message blocks (102) and log records (104) in conjunction with single file disk storage that allows the write head never to have to back-up to traverse saved data when writing new records. The system also permits locating damaged files without the requirement of scanning entire log files.

French Abstract
La presente invention concerne un systeme de gestion de files d'attente de messages permettant de sauvegarder et de stocker des messages et leurs etats dans un fichier unique efficace residant sur un seul disque de facon a recuperer rapidement les defaillances d'un serveur. Le systeme de stockage monodisque monofichier, dans lequel des messages et leurs etats sont stockes, permet d'eliminer des operations d'ecriture sur trois disques differents: le disque de donnees, le disque de structure d'index et le disque de journalisation. Le stockage monodisque monofichier est rendu possible par le regroupement des informations dans un espace contigu sur le meme disque. Toutes les operations d'ecriture sont, donc, effectuees en un seul mouvement de balayage de la tete de lecture qui se deplace dans un seul sens et une seule fois de facon a trouver la zone dans laquelle elle doit commencer a ecrire des messages et stocker leurs etats. Pour conserver une trace des informations regroupees, on utilise une seule table de correspondance d'entree de mise en file d'attente (100) comportant des informations de gestion (100), des blocs de messages (102) et des articles de journalisation (104) conjointement avec un stockage sur disque monofichier permettant a la tete de lecture de ne jamais avoir, a des fins de sauvegarde, a faire defiler des donnees sauvegardees lors de l'ecriture de nouveaux articles. Le systeme permet, egalement, de localiser des fichiers endommages sans qu'il soit necessaire de balayer la totalite des fichiers de journalisation.

00418748 **Image available**

**SYSTEMS AND METHODS FOR SECURE TRANSACTION MANAGEMENT AND ELECTRONIC RIGHTS PROTECTION**

**SYSTEMES ET PROCEDES DE GESTION DE TRANSACTIONS SECURISEES ET DE PROTECTION DE DROITS ELECTRONIQUES**

Patent Applicant/Assignee:
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Inventor(s):
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SHEAR Victor H,
SIBERT W Olin,
SPAHN Francis J,
VAN WIE David M,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9809209 A1 19980305
Application: WO 97US15243 19970829 (PCT/WO US9715243)
Priority Application: US 96706206 19960830
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: **G06F-001/00**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 195626

English Abstract

The present invention provides systems and methods for electronic commerce including secure transaction management and electronic rights protection. Electronic appliances such as computers employed in accordance with the present invention help to ensure that information is accessed and used only in authorized ways, and maintain the integrity, availability, and/or confidentiality of the information. Secure subsystems used with such electronic appliances provide a distributed virtual distribution environment (VDE) that may enforce a secure chain of handling and control, for example, to control and/or meter or otherwise monitor use of electronically stored or disseminated information. Such a virtual distribution environment may be used to protect rights of various participants in electronic commerce and other electronic or electronic-facilitated transactions. Secure distributed and other operating system environments and architectures, employing, for example, secure semiconductor processing arrangements that may establish secure, protected environments at each node. These techniques may be used to support an end-to-end electronic information distribution capability that may be used, for example, utilizing the "electronic highway".

French Abstract

La presente invention concerne des systemes et des procedes de commerce electronique comprenant une gestion de transactions securisees et la protection de droits electroniques. Des appareils electroniques tels que des ordinateurs utilises conformement a la presente invention contribuent a assurer que l'acces aux informations et l'utilisation des informations ne se font que par des voies autorisees et ils maintiennent l'integrite, la disponibilite et/ou la confidentialite des informations. Des sous-systemes securises utilises avec ces appareils electroniques constituent un environnement de distribution virtuel (VDE) reparti pouvant faire valoir une chaine securisee de traitement et de commande, par exemple, pour commander et/ou mesurer ou encore controler l'utilisation d'informations memorisees ou disseminees electroniquement. Cet environnement de distribution virtuel peut etre utilise pour proteger les droits de divers participants dans le commerce electronique et dans d'autres transactions electroniques ou dans lesquelles intervient l'electronique. Des environnements et des architectures de systemes

repartis securises et autres systemes d'exploitation emploient, par exemple, des arrangements de traitement a semi-conducteurs securises pouvant etablir des environnments proteges securises a chaque noeud. On peut utiliser ces techniques pour apporter un soutien a une capacite de distribution d'informations electroniques de bout-en-bout pouvant etre utilisees, par exemple, en empruntant l'"autoroute electronique".

**15/5/23 (Item 23 from file: 349)**



00401839 **Image available**

**SYSTEM AND METHOD FOR GENERATING FRACTIONAL LENGTH DELAY LINES IN A DIGITAL SIGNAL PROCESSING SYSTEM**

**SYSTEME ET PROCEDE DE PRODUCTION DE LIGNES FRACTIONNELLES A RETARD EN DISTANCE, DANS UN SYSTEME DE TRAITEMENT DE SIGNAUX NUMERIQUES**

Patent Applicant/Assignee:
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JAFFE David A,
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Patent and Priority Information (Country, Number, Date):
Patent: WO 9742583 A1 19971113
Application: WO 97US5610 19970403 (PCT/WO US9705610)
Priority Application: US 96647296 19960509
Designated States: AU CA JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-017/17**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 6420

English Abstract

A sampled data, non-integer delay line interpolation structure (150) includes a sampled data delay line (156), two allpass filters (162, 164), each having an associated read pointer (158, 160) for reading data at a corresponding integer position of the delay line, an alternating crossfader (166) that alternatingly crossfades between the outputs of the two allpass filters, plus a controller (154) that controls when the read position of each allpass filter is updated and also controls when the filter coefficient of each allpass filter is updated. A specified delay length value is sampled by the controller each time the crossfade orientation of the alternating crossfader is changed, and from that value the controller generates a new read pointer and filter coefficient for allpass filter to which the structure will next crossfade.

French Abstract

On decrit une structure (150) d'interpolation de lignes a retard, non entieres et contenant des donnees echantillonnees, laquelle structure comprend une ligne (156) a retard contenant des donnees echantillonnees, deux filtres passe-tout (162, 164) possedant chacun un pointeur de lecture (158, 160), aux fins de lecture de donnees au niveau d'une position entiere correspondante de la ligne a retard, un dispositif de fondu-enchaine (166) qui execute un fondu-enchaine de facon alternee entre les sorties des deux filtres passe-tout, ainsi qu'un dispositif de temporisation (154), destine a commander quand la position de lecture de chaque filtre est a mettre a jour et egalement quand le coefficient de filtre de chaque filtre est a mettre a jour. Ce dispositif de temporisation echantillonne une valeur de distance de retard specifiee, lors de chaque changement d'orientation du fondu-enchaine du dispositif d'execution alternee des fondus-enchaines, et a partir de cette valeur, il produit un nouveau pointeur de lecture et un nouveau coefficient de filtre pour le filtre en fonction desquels la structure va executer le

fondu-enchaine.

**15/5/24 (Item 24 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT


00374258
**RISC MICROPROCESSOR ARCHITECTURE**
**ARCHITECTURE DE MICROPROCESSEUR RISC**
Patent Applicant/Assignee:
PATRIOT SCIENTIFIC CORPORATION,
SHAW George W,
McCLURG Martin G,
JENSEN Bradley D,
FISH Russel H III,
MOORE Charles H,
Inventor(s):
SHAW George W,
McCLURG Martin G,
JENSEN Bradley D,
FISH Russel H III,
MOORE Charles H,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9715001 A2 19970424
Application: WO 96US16013 19961004 (PCT/WO US9616013)
Priority Application: US 955408 19951006
Designated States: JP US AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-009/22**
International Patent Class: **G06F-12:04 ; G06F-03:00**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 49725

English Abstract
MPU (108) contains 52 general-purpose registers, including 16 global data registers (104), an index register (132), a count register (134), a 16-deep addressable register/return stack (124), and an 18-deep operand stack (122). Both stacks contain an index register (128, or 130) in the top elements, are cached on chip, and, when required, automatically spill to and refill from external memory. The stacks minimize the data movement and also minimize memory access during procedure calls, parameter passing, and variable assignments. Additionally, the MPU contains a mode/status register (136) and 41 locally addressed registers (102) for I/O, control, configuration, and status. The CPU (100) contains both a high-performance, zero-operand, dual-stack architecture microprocessing unit (MPU) (108), and an input-output processor (IOP) (110) that executes instructions to transfer data, count events, measure time, and perform other timing-dependent functions.

French Abstract
Ce microprocesseur (100) execute les instructions avec des performances de pointe de 100 millions d'instructions par seconde (MIPS) en mode naturel, a une frequence de base interne de 100 MHz. Les jeux d'instructions de l'unite centrale sont cables, ce qui permet a la majorite des instructions de s'executer en un seul cycle. Une conception de circulation permet a l'instruction suivante de demarrer avant que l'instruction precedente ne soit terminee, ce qui ameliore les performances du systeme. Une unite microprocesseur (108) contient 52 registres a usages multiples, comprenant 16 registres de donnees communs (104), un registre d'index (132), un registre de comptage (134), une pile de retour/ registres adressables (124), d'une profondeur de 16 registres et une pile d'operandes (122) d'une profondeur de 18 operandes. Les deux piles contiennent un registre d'index (128) ou (130) dans les elements superieurs, sont mises en antememoire sur une puce, et, le cas echeant, se deversent automatiquement dans une memoire externe et sont a nouveaux

remplies a partir de cette memoire. Les piles reduisent au minimum le mouvement des donnees ainsi que l'acces en memoire au cours d'appels de traitement, de la transmission de parametres et d'affectations variables. En outre, le microprocesseur contient un registre de mode/d'etat (136) et 41 registres (102) a adressage local pour les fonctions d'E/S, de commande, de configuration et d'etat. L'unite centrale (100) contient a la fois une unite microprocesseur (MPU) performante a architecture a double pile et zero operande (108), et un processeur d'entree-sortie (IOP) (110) qui execute des instructions pour transferer des donnees, compter des evenements, compter le temps, et executer d'autres fonctions dependantes de la synchronisation. Une architecture (a pile) a zero operande permet de supprimer les bits d'operande. Les piles reduisent egalement au minimum les sauvegardes et les chargements en registre au cours d'un traitement et d'un traitement a l'autre, permettant ainsi d'utiliser des sequences d'instructions plus courtes et un code a execution plus rapide. Les instructions sont faciles a decoder et a executer, permettant ainsi au MPU (108) et au IOP (110) d'emettre et de terminer les instructions dans un seul cycle d'horloge, chacun a une execution de pointe de 100 MIPS en mode naturel. L'unite centrale (100), en faisant appel a des codes d'operation a 8 bits, obtient jusqu'a quatre instructions de la memoire a chaque fois qu'une extraction ou une pre-extraction d'instructions est realisee. Ces instructions peuvent etre repetees sans qu'elles ne doivent etre relues dans la memoire. Ceci permet au systeme de rester performant lorsqu'il est directement connecte a une memoire RAM dynamique, sans antememoire.

**15/5/25 (Item 25 from file: 349)**



00344642

**SYSTEMS AND METHODS FOR SECURE TRANSACTION MANAGEMENT AND ELECTRONIC RIGHTS PROTECTION**

**SYSTEMES ET PROCEDES DE GESTION SECURISEE DE TRANSACTIONS ET DE PROTECTION ELECTRONIQUE DES DROITS**

Patent Applicant/Assignee:
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SPAHN Francis J,
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Patent and Priority Information (Country, Number, Date):
Patent: WO 9627155 A2 19960906
Application: WO 96US2303 19960213 (PCT/WO US9602303)
Priority Application: US 95388107 19950213
Designated States: AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN KE LS MW SD SZ UG AZ BY KG KZ RU TJ TM AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: **G06F-001/00**
International Patent Class: **G06F-17:60**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 207972

English Abstract
The present invention provides systems and methods for electronic commerce including secure transaction management and electronic rights protection. Electronic appliances such as computers employed in accordance with the present invention help to ensure that information is accessed and used only in authorized ways, and maintain the integrity, availability, and/or confidentiality of the information. Secure subsystems used with such electronic appliances provide a distributed

virtual distribution environment (VDE) that may enforce a secure chain of handling and control, for example, to control and/or meter or otherwise monitor use of electronically stored or disseminated information. Such a virtual distribution environment may be used to protect rights of various participants in electronic commerce and other electronic or electronic-facilitated transactions. Secure distributed and other operating system environments and architectures, employing, for example, secure semiconductor processing arrangements that may establish secure, protected environments at each node. These techniques may be used to support an end-to-end electronic information distribution capability that may be used, for example, utilizing the "electronic highway".

French Abstract

Systemes et procedes destines au domaine du commerce electronique, et notamment a la gestion securisee des transactions et a la protection electronique des droits. Les appareils electroniques tels que les ordinateurs utilises conformement a la presente invention permettent d'assurer que les informations ne sont consultees et exploitees que de maniere autorisee, et ils conservent l'integrite, la disponibilite et/ou le caractere confidentiel des informations. Les sous-systemes securises utilises en association avec de tels appareils electroniques constituent un environnement de distribution virtuel distribue (VDE) apte a imposer une chaine securisee de traitement et de commande, par exemple pour la commande et/ou la mesure ou encore le controle de l'utilisation d'informations stockees ou diffusees electroniquement. Cet environnement de distribution virtuel peut servir a proteger les droits de differents individus impliques dans le commerce electronique et dans d'autres transactions electroniques ou assistees par des moyens electroniques. On a egalement prevu des environnements et architectures de systeme d'exploitation distribues, securises et autres mettant en oeuvre, par exemple, des ensembles de traitement securise a semi-conducteurs pouvant etablir des environnements securises et proteges au niveau de chaque noeud. Ces techniques peuvent servir de soutien pour une fonction electronique de distribution d'informations de bout en bout, cette fonction etant utilisable, par exemple, dans le domaine de l'"autoroute electronique".

**15/5/26 (Item 26 from file: 349)**



00253670 **Image available**

**A SINGLE CHIP INTEGRATED CIRCUIT SYSTEM ARCHITECTURE FOR VIDEO-INSTRUCTION-SET-COMPUTING**

**ARCHITECTURE DE CIRCUIT INTEGRE MONOPUCE POUR LE CALCUL PAR JEUX D'INSTRUCTIONS VIDEO**

Patent Applicant/Assignee:
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SHAW Steven M,
Inventor(s):
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SHAW Steven M,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9401824 A1 19940120
Application: WO 93US5863 19930617 (PCT/WO US9305863)
Priority Application: US 92909312 19920706
Designated States: AT AU BB BG BR CA CH DE DK ES FI GB HU JP KP KR LK LU MG MN MW NL NO PL RO RU SD SE US AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: **G06F-015/21**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 24238

English Abstract

The present invention pertains to integrated circuit system based on novel architecture of Video-Instruction-Set-Computing (VISC). The integrated circuit comprises a plurality of functional units to independently execute the tasks of remote communication, bandwidth adaptation, application control, multimedia management, and universal video encoding. The integrated circuit is also comprised of scalable formatter element connecting to the functional units which can inter-operate arbitrary external video formats and intelligently adapt to selective internal format depending upon the system throughput and configuration. Additionally, there is a smart memory element connecting to the functional units and scalable formatter, which can access, store, and transfer blocks of video data based on selective internal format. In the preferred embodiment, the integrated circuit is also comprised of an embedded RISC or CISC co-processor element in order to execute DOS, Windows, NT, Macintosh, OS2, or UNIX applications. In a more preferred embodiment, the integrated circuit includes a real time object oriented operation system element wherein concurrent execution of the application program and real time VISC based video instruction sets can be performed. The present invention is designed to sustain the evolution of a plurality of generations of the VISC microprocessors. These novel VISC microprocessors can be efficiently used to perform wide range of real time distributed video signal processing functions for applications such as interactive video, HDTV, and multimedia communications.

French Abstract

L'invention concerne un systeme de circuit integre concu d'apres une nouvelle architecture de calcul par jeux d'instructions video (VISC). Le circuit integre se compose d'une pluralite d'unites fonctionnelles qui executent independamment les taches de communication a distance, d'adaptation de la largeur de bande, de controle d'application, de gestion de supports multiples, et de codage video universel. Ledit circuit integre se compose egalement d'un element formateur variable reliant aux unites fonctionnelles qui peuvent interfonctionner avec des formats video externes arbitraires et s'adapter de maniere intelligente au format interne selectif selon la capacite utile du systeme et sa configuration. On utilise en outre un element memoire intelligent relie aux unites fonctionnelles et au formateur variable, qui peut acceder a des blocs de transfert de donnees videos basees sur le format interne selectif et les stocker. Dans le mode prefere de realisation, ledit circuit integre se compose egalement d'un element coprocesseur RISC ou CISC integre concu pour executer des applications DOS, Windows, NT, Macintosh, OS2 ou UNIX. Dans un mode de realisation encore plus avantageux, le circuit integre se compose d'un systeme d'exploitation oriente d'objet en temps reel dans lequel l'execution du programme d'application peut s'effectuer en meme temps que celle des jeux d'instructions videos en temps reel a base VISC. Le systeme selon l'invention permet de supporter l'evolution d'une pluralite de generations de microprocesseurs VISC. Ces nouveaux microprocesseurs VISC peuvent etre utilises de maniere efficace pour effectuer une gamme etendue de fonctions de traitement de signaux video distribues en temps reel pour des applications telles que la video interactive, la television haute definition, et les communications multimedia.

**15/5/27 (Item 27 from file: 349)**



00211830

**COMPUTER WITH TABLET INPUT TO STANDARD PROGRAMS**

**ORDINATEUR COMPRENANT UNE ENTREE PAR NUMERISEUR POUR DES PROGRAMMES STANDARD**

Patent Applicant/Assignee:
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HUNTINGTON Jonathan T II,
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BARRETT David M,
WARD Jean Renard,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9209037 A1 19920529
Application: WO 91US4460 19910620 (PCT/WO US9104460)
Priority Application: US 90324 19901113
Designated States: AT AU BE CA CH DE DK ES FR GB GR IT JP LU NL SE
Main International Patent Class: **G06F-015/02**
International Patent Class: **G06F-03:033**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 21971

English Abstract
A computer system having a digitizing tablet overlaying the display screen. The tablet serves as a user's primary input device. Various features of the system make it possible for the user to run and interact with standard programs designed for keystroke and mouse input and not designed for use with a tablet. In addition to the main processor, on which the user's programs are executed, there is an interface processor. In addition to a standard display buffer, there is an ink plane buffer for interface display data that is combined with the data from the standard display buffer on a pixel-by-pixel basis according to data from a mask plane buffer. The interface processor manages input from the tablet, presents feedback to the user by means of the ink and mask planes, and provides keystroke and mouse data to the main processor as if from a standard keyboard controller. The interface processor presents the user with a collection of simulated devices, including standard devices such as a keyboard and a mouse. A nonstandard simulated device performs character recognition, permitting handwritten characters to be used for program input. During interaction with one of the user's programs, the user can activate and deactivate simulated devices (by removing them from and returning them to a device tray) and can make adjustments in their operation and location on the screen.

French Abstract
Systeme informatique comprenant un numeriseur recouvrant l'ecran de visualisation. Plusieurs fonctions du systeme permettent a l'utilisateur d'executer des programmes standard et de dialoguer avec ces derniers qui sont concus pour etre introduits par l'intermediaire d'un clavier ou d'une souris et qui ne sont pas destines a etre utilises avec un numeriseur. En outre, un processeur d'interface vient s'ajouter au processeur principal, dans lequel les programmes de l'utilisateur sont executes. Hormis l'affichage intermediaire standard, il existe un tampon a ecran a encre pour les donnees d'affichage de l'interface qui sont associees aux donnees provenant de l'affichage intermediaire standard sur une base pixel par pixel en fonction des donnees provenant d'un tampon de plan a masque. Le processeur d'interface gere l'entree provenant du numeriseur, presente la retroaction a l'utilisateur a l'aide des plans a masque et a encre, et fournit au processeur principal des donnees de clavier et de souris de la meme maniere que si elles provenaient d'une commande par clavier standard. Le processeur d'interface presente a l'utilisateur un ensemble de dispositifs simules comprenant des dispositifs standards tels qu'un clavier et une souris. Un dispositif simule special effectue la reconnaissance des caracteres, ce qui permet d'utiliser des caracteres manuscrits pour entrer des programmes. Lorsque l'utilisateur dialogue avec un de ses programmes, il peut lancer ou arreter des dispositifs simules en les sortant d'un chariot de dispositifs ou bien en les renvoyant vers ce dernier et il peut egalement effectuer des modifications au niveau de leur fonctionnement et de leur emplacement sur l'ecran.

**15/5/28 (Item 28 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT

00106554 **Image available**

**DATA PROCESSING SYSTEM**

**SYSTEME DE TRAITEMENT DE DONNEES**

Patent Applicant/Assignee:
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Inventor(s):
COLLEY S,
RATTNER J,
COX G,
SWANSON R,

Patent and Priority Information (Country, Number, Date):
Patent: WO 8102477 A1 19810903
Application: WO 80US205 19800228 (PCT/WO US8000205)
Priority Application: WO 80US205 19800228
Designated States: DE GB JP AT CH DE FR GB LU NL SE
Main International Patent Class: **G06F-003/00**
International Patent Class: **G06F-07:00** ; **G06F-09:00** ; **G06F-13:00** ; **G06F-15:16** ; **G06F-15:20**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 139912

English Abstract

A data processor architecture wherein the processors recognize two basic types of objects, an object being a representation of related information maintained in a contiguously addressed set of memory locations. The first type of object contains ordinary data, such as characters, integers, reals, etc. The second type of object contains a list of access descriptors. Each access descriptor provides information for locating and defining the extent of access to an object associated with that access descriptor. The processors recognize complex objects that are combinations of objects of the basic types. One such complex object (94) defines an environment (18 or 20) for execution of objects (92, 93, 98, 106, 122) accessible to a given instance of a procedural operation. The dispatching of tasks to the processor is accomplished by hardware-controlled queuing mechanisms (36), dispatching-port objects (146) which allow multiple sets of processors (38) and (40) to serve multiple, but independent sets of tasks (14, 16). Communication between asychronous tasks or processes is accomplished by related hardware controlled queuing mechanisms (34) (buffered-port objects) (144) which allow messages to move between internal processes or input/output processes without the need for interrupts. A mechanism (42) is provided which allows the processors to communicate with each other. This mechanism is used to reawaken an idle processor to alert the processor to the fact that a ready-to-run process at a dispatching port needs execution.

French Abstract

Structure de processeur de donnees dans laquelle les processeurs reconnaissent deux types fondamentaux d'objets, un objet etant constitue par une representation d'informations connexes maintenues dans un groupe d'emplacements de memoire adresse en contiguite. Le premier type d'objets contient des donnees ordinaires, telles que des caracteres, des nombres entiers, reels, etc. Le deuxieme type d'objets contient une liste de descripteurs d'acces. Chaque descripteur d'acces fournit une information servant a localiser et definir l'etendue de l'acces a un objet associe a ce descripteur. Les processeurs reconnaissent des objets complexes constitues par des combinaisons d'objets des types fondamentaux. Un tel objet complexe (94) definit un environnement (18) ou (20) pour l'execution d'objets (92, 93, 98, 106, 122) accessible a un moment donne d'une operation de traitement. La repartition des taches aux processeurs est executee par des mecanismes (36) de mise en file d'attente commandes par le materiel, des objets (146) de points de connexion de repartition permettant a des groupes multiples de processeurs (38 et 40) d'executer des ensembles de taches (14, 16) multiples mais independantes. La

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Set     Items   Description
S1       3585   API OR APPLICATION()PROGRAM?()INTERFACE? OR (APPLICATION? -
            OR PROGRAM?)(2W)INTERFACE?
S2        101   (TIME()DEPENDENT? OR SYNCHRON?) AND (ASYNCHRON? OR (NON OR
            "NOT")()SYNCHRONOUS)
S3       1266   TIMER? OR TIMING OR TIMESTAMP? OR INTERVAL? OR CLOCK?
S4      12673   END? ? OR TIMEOUT? OR TIME()OUT? ? OR EXPIR?
S5          7   S3(3N)(DATABASE? OR DATA()(BASE? OR BANK? OR FILE?) OR DAT-
            ABANK? OR DATAFILE? OR TABLE?)
S6        921   STATEMACHINE? OR STATE()MACHINE? OR CONTROLLER?
S7          2   INITILIALI? OR REINITIALI?
S8         96   S3(3N)(MANAG? OR CONTROL? OR ADMINIST? OR MONITOR? OR TRAC-
            K?)
S9         12   S1 AND S2
S10         4   S9 AND S3
S11         0   S9 AND (S6 OR S7 OR S4)
S12         4   S10 NOT PY>2000
S13         4   S12 NOT PD>20000928
File 256:SoftBase:Reviews,Companies&Prods. 82-2003/Feb
         (c)2003 Info.Sources Inc
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13/3,K/1
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.


01707333 DOCUMENT TYPE: Product

**PRODUCT NAME: Ventura (707333)**

Innovative Integration (643815)
5785 Lindero Canyon Rd
Westlake Village, CA 91362 United States
TELEPHONE: (818) 865-6150

RECORD TYPE: Directory

CONTACT: Sales Department

REVISION DATE: 19981030

...with a host PC at millions of bytes per second. Simultaneously, users' application programs can **asynchronously** access other board peripheral resources to perform digital I/O, read counters, reprogram **timer** channels, and perform sync serial communications at rates to several kilohertz. The software is packaged as a Windows DLL, employing an elegant, simple **application programming interface** ( **API** ). It can be readily accessed from within any popular PC programming environment, including Visual C...

...and analysis of real-time analog or digital signals within a single environment. The Ventura **API** (VAPI) provides control over **synchronous** and **asynchronous** operations. **Asynchronous** functions include configuration, control and real-time, non- streaming hardware access activities. **Synchronous** functions control continuous analog capture and playback modes. Configuration is easy, using a single software...

...running at the full bandwidth of the target hardware. The code is interrupt- driven, allowing **asynchronous** commands to be executed during streaming acquisition making it ideal for applications involving a mix...

13/3,K/2
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.


01124991 DOCUMENT TYPE: Product

**PRODUCT NAME: WinSpec (124991)**

Roper Scientific Inc (730165)
3440 E Britannia Dr
Tucson, AZ 85706 United States
TELEPHONE: (520) 889-9933

RECORD TYPE: Directory

CONTACT: Sales Department

REVISION DATE: 021231

...the features of Roper Scientific digital imaging and spectroscopy hardware. Employing the PVCAM (R) universal **programming interface** , WinSpec controls all Roper Scientific detectors, regardless of sensor format or architecture. The system provides users with access to sensor readout and **timing** data. A straightforward interface streamlines parameter configuration processes. A **synchronous** acquisition mode allows users to collect high frame-rate data. **Asynchronous** acquisition works well for system configuration, as well as for initial and time-lapse data ...

...displays 2D and 3D graphs. It includes zooming, scaling, and cross-section viewing features. The **program** 's **interface** can be customized. WinSpec supports a wide range of programmable **timing** generators. The Step-and-Glue feature allows users to combine multiple high-resolution spectra. Macro...

**13/3,K/3**
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.


00110042 DOCUMENT TYPE: Review

**PRODUCT NAMES: POSIX (830174)**

**TITLE: Real Time Goes Mainstream**
AUTHOR: Friesenhahn, Bob
SOURCE: Byte, v23 n7 p39(2) Jul 1998
ISSN: 0360-5280
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RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

REVISION DATE: 20010730

IEEE's POSIX.4 was developed to redefine Posix **application programming interfaces** (APIs) and to develop new APIs to meet the needs of real-time environments. To...

...for efficient communications, APIs were added that support memory mapping, message queues, semaphores, signals, and **asynchronous** I/O; in addition existing calls were extended, and **timers** , memory locking, and programmable scheduling abilities were added to allow precise **timing** and scheduling required **time - dependent** tasks. Many legacy OSs provided some of these features, but not in a quick and...

...Mmap is very robust, with the ability to map memory among processes. Posix.4's **asynchronous** I/O allows an application to continue execution and be notified when the operation is...

**13/3,K/4**
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.


00088588 DOCUMENT TYPE: Review

**PRODUCT NAMES: POSIX (830174)**

**TITLE: Posix has leading role in open system**
AUTHOR: Singh, Inder M
SOURCE: Electronic Engineering Times, v881 p54(2) Dec 18, 1995
ISSN: 0192-1541
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RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

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...embedded real-time design world toward open systems. POSIX 1003.1 defines a standard UNIX **application programming interface** ( **API** ), and POSIX.1b extensions specify cover areas, such as priority scheduling, shared memory, improved **timer** support, extended reliable signals, and

**synchronized** or true **asynchronous** I/O. POSIX.1c facilities are for support of multiple execution threads through concurrent and **asynchronous** activities that intercommunicate shared data frequently. POSIX 1003.13 specifies profiles for different classes of..